1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2009-05-19

SCHEMATIC,"ANGEL ISLAND",MLB

Rev.A 02/23/10

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8503	1	SCHEM,ANGEL_ISLAND,MLB,K17	SCH	CRITICAL	
820-2849	1	PCBF,ANGEL_ISLAND,MLB,K17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 23 21:52:40 2010

DRAWING TITLE

Apple Inc.

DRAWING NUMBER | SIZE D

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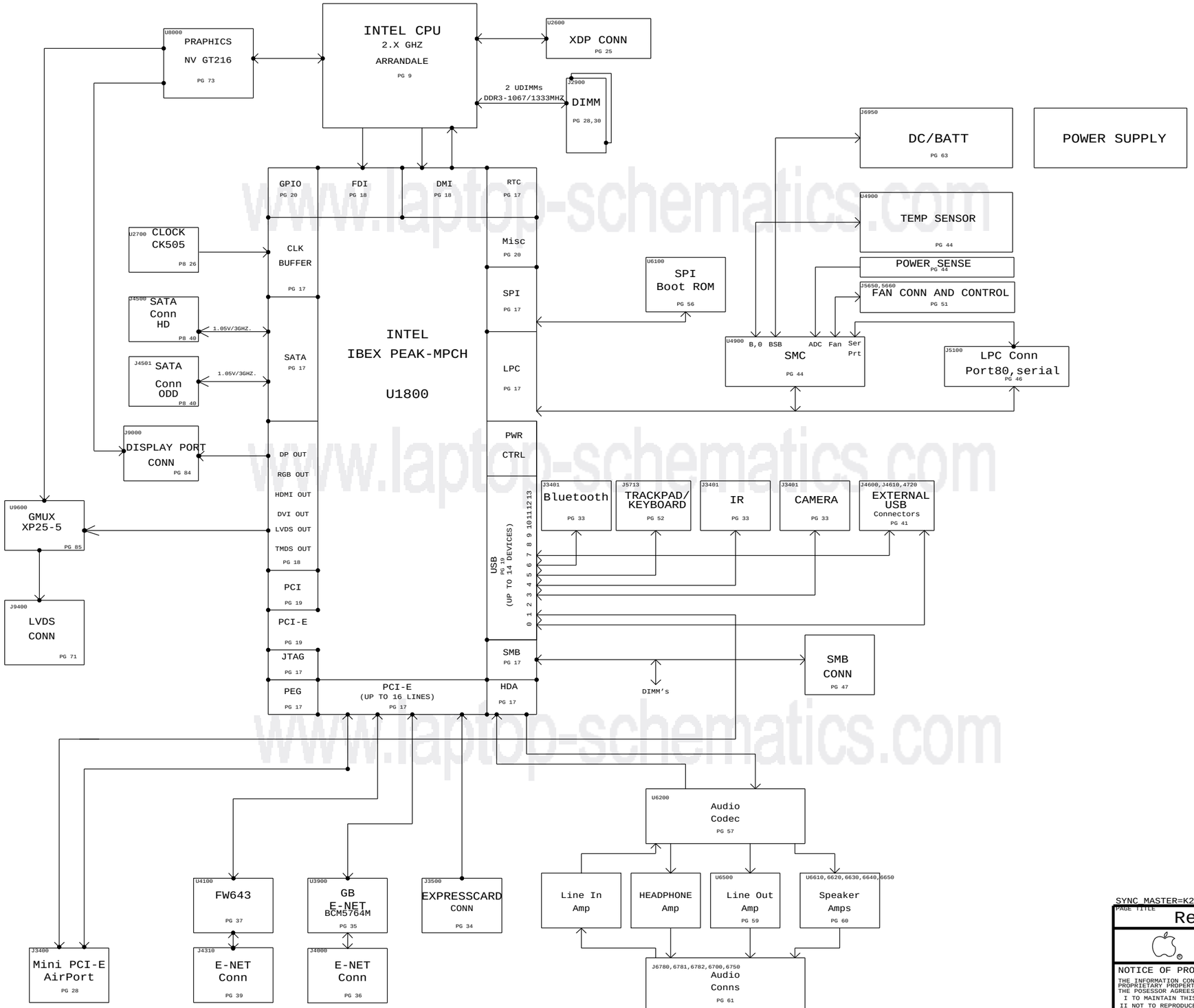

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: Revision History

Apple Inc.

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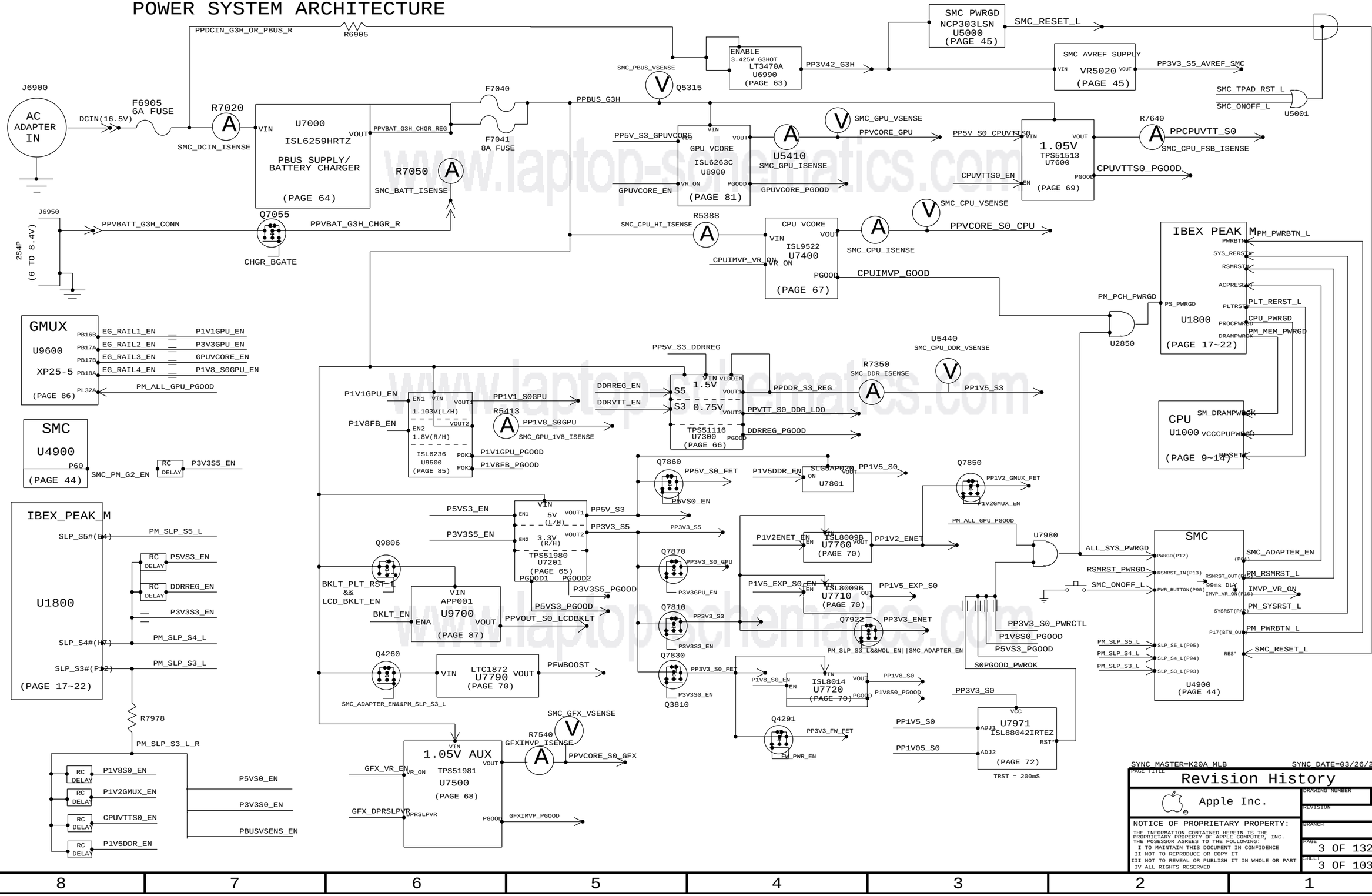
POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

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Apple Inc.

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(For changes prior to Rev. A, refer to earlier schematics)

Rev. A:

02/23/10
MLB_TI_IMVP65
csa. 5 Added K17_PVT BOM group
csa. 74 Updated Symbol for U7400; new VPN is TPS51983
csa. 121 Changed ARB_ONLY sense Rs to XWs

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

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Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0973	PCBA,2.53GHZ,512SAM_VRAM,K17	K17_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,EEEE_DCMV,K17_PVT
639-0971	PCBA,2.53GHZ,512HYN_VRAM,K17	K17_COMMON,CPU_2_53GHZ,FB_512_HYNIX,EEEE_DCMR,K17_PVT
639-0972	PCBA,2.66GHZ,512SAM_VRAM,K17	K17_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,EEEE_DCMT,K17_PVT
639-0970	PCBA,2.66GHZ,512HYN_VRAM,K17	K17_COMMON,CPU_2_66GHZ,FB_512_HYNIX,EEEE_DCMQ,K17_PVT
085-1425	K17 MLB DEVELOPMENT	K17_DEVEL_ENG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
516S0806	516S0805		ALL	FOXCONN ALT TO MOLEX
138S0612	138S0602		ALL	Taiyo Yuden alt to Samsung
353S2805	353S2603		ALL	Fairchild 8 in alt to 6 in wafer
127S0111	127S0060		ALL	Rohm alt to Kemet
128S0299	128S0218		ALL	NEC/TOKIN alt to Sanyo
337S3808	337S3839		ALL	GT216 A02 alt to A03 part
376S0887	376S0749		ALL	Fairchild alt to Vishay

K17 BOM GROUPS

BOM GROUP	BOM OPTIONS
K17_COMMON	ALTERNATE,COMMON,K17_COMMON1,K17_COMMON2,K17_PROGPARTS
K17_COMMON1	BCM5764M,DCI,GMUX_VSYNC,CPUPOC_IMAX_40_50,PCH_NAND_3V3,CPUMEM_S0,EXT_HP_AMP,VFRQ_SLPS3,SMC_DEBUG_YES,DPMUX_EN_PLD,FB1V35,USBHUB_2061
K17_COMMON2	GPUVID_0P90V,BKLT_PWR_PBUS,DP_ESD,DP_CA_DET_EG_PLD,SMC_EXCARD_NOT,GPU_SS_INT,RDRV_8515_A2,GMUXPLL_3V3,HUB1_2NONREM,HUB2_2NONREM,RAIL_MON
K17_DEVEL_ENG	ARB_ONLY,CALPELLA_XDP,DEBUG_ADC,LPCPLUS,VREFMRGN,GMUX_JTAG_CONN,EFI_DEBUG,BMON_ENG,SMC_OSC_YES
K17_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG
K17_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM

BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX
CALPELLA_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_NORMAL,XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMQ]	CRITICAL	EEEE_DCMQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMR]	CRITICAL	EEEE_DCMR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMT]	CRITICAL	EEEE_DCMT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCMV]	CRITICAL	EEEE_DCMV

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3847	1	ARD,SLBPF,PRQ,2.53,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3848	1	ARD,SLBPE,PRQ,2.66,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3846	1	ARD,SLBNA,PRQ,2.40,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IBEX (HM55),SLGZS,PRQ,B3	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8X8,64 QFN	U3900	CRITICAL	BCM5764M
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0229	1	IC,SMC,K17	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341T0244	1	IC,EFI ROM,K17	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,TP PSOC,K17,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2568	1	IC,CPLD,LATTICE,132CSBGA,K17MLB	U9600	CRITICAL	GMUX_PROG
333S0533	4	IC,SGRAM,GDDR3,32MX32,1GHZ,D-DIE,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,900MHZ,TIVA,HF	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX
341S2731	1	IC,1MBIT,SPI FLASH K17/K18	U3990	CRITICAL	
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,NON/SC	J3100	CRITICAL	
197S0350	1	OSC,XTAL,32.768KHZ,9-3.6V,12P SOIC,HF	U5010	CRITICAL	SMC_OSC_YES

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: BOM Configuration

Apple Inc.

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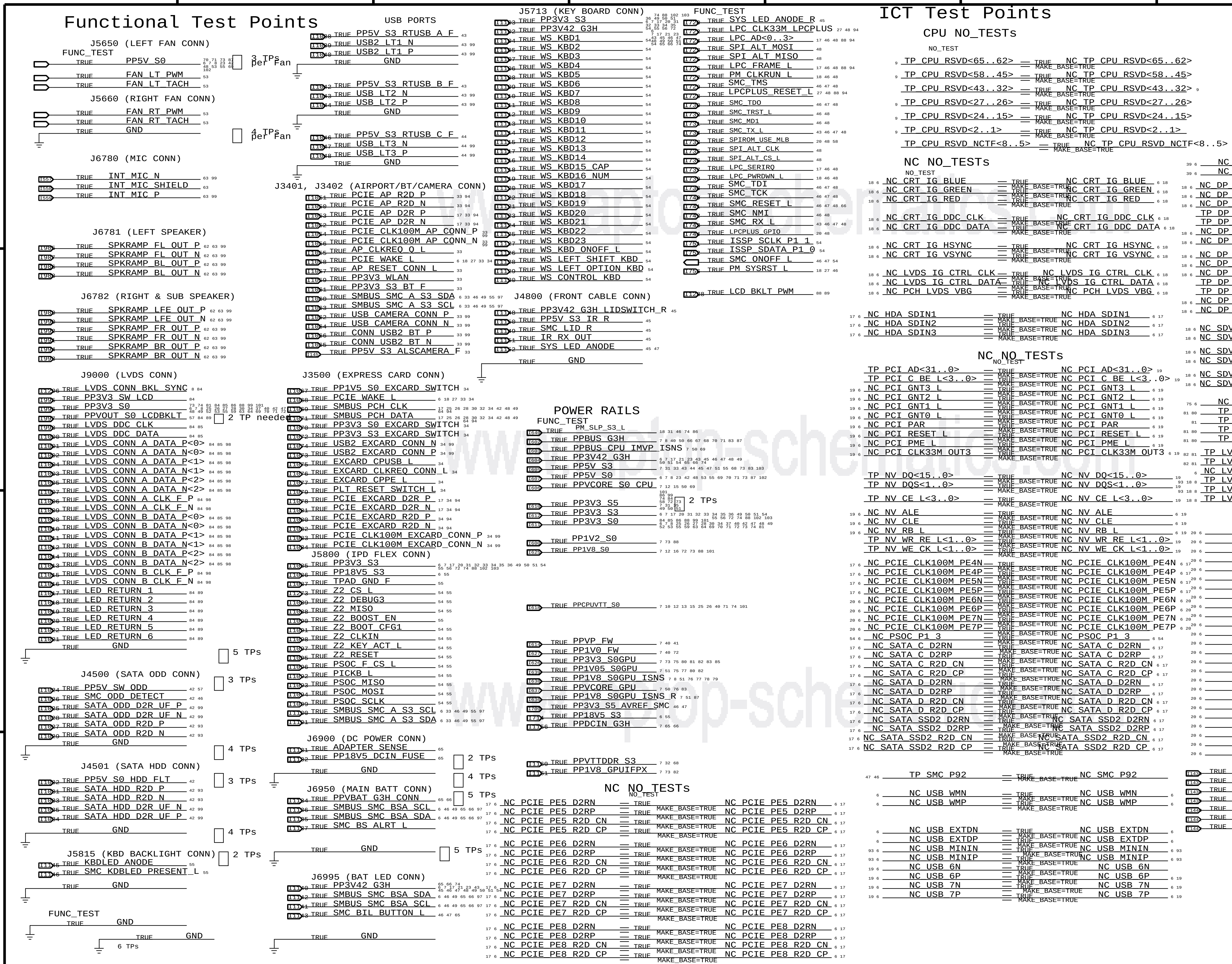

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

PAGE TITLE

Functional / ICT Test

Apple Inc.

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
PPBUS_CPU_IMVP_ISNS
PPDCIN_G3H
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=15.6V
MAKE_BASE=TRUE
PPDCIN_G3H
PP3V42_G3H
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H
PP3V42_G3H

5V Rails

PP5V_S5
PP5V_S5
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S5
PP5V_S5
PP5V_S5
PP5V_S5
PP5V_S5
PP5V_S5
PP5V_S3
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3
PP5V_S3_ISNS_R
PP5V_S3_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S3_ISNS_R
PP5V_S0
PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0
PP5V_S0_ISNS_R
PP5V_S0_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
PP5V_S0_ISNS_R

3.3V/1.8V Rails

PP3V_S5
PP3V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5
PP3V3_S5_ISNS_R
PP3V3_S5_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S5_ISNS_R
PP3V3_S3
PP3V3_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3_ISNS_R
PP3V3_S3_ISNS_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S3_ISNS_R
PP3V3_S0
PP3V3_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP3V3_S0
PP1V8_S0
PP1V8_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0
PP1V8_S0
PP1V8_S0
PP1V8_S0

DDR Rails

PP1V5_S3
PP1V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3
PP1V5_S3
PP1V5_S3
PP1V5_S3
PP1V5_S3
PP1V5_S3RS0
PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S3RS0
PPCPUDDR_ISNS
PPCPUDDR_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPCPUDDR_ISNS
PPCPUDDR_ISNS
PPVTTDDR_S3
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PPVTTDDR_S3
PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT
PP0V75_S0_DDRVTT

1.5V/1.05V Rails

PP1V5_S0
PP1V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V2_S0
PP1V2_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S0
PP1V05_S5
PP1V05_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S5

Chipset "VCore" Rails

PPVCORE_S0_CPU
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU
PPVCORE_S0_GFX
PPVCORE_S0_GFX
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPVCORE_S0_GFX
PPVCORE_S0_CPU_VCAP0
PPVCORE_S0_CPU_VCAP0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PPVCORE_S0_CPU_VCAP1
PPVCORE_S0_CPU_VCAP1
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PPVCORE_S0_CPU_VCAP2
PPVCORE_S0_CPU_VCAP2
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

ENET Rails

PP3V3_ENET
PP3V3_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_ENET
PP1V2_ENET
PP1V2_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_ENET
PP1V2_ENET

"FW" (FireWire) Rails

PPBUS_FW_FWBOOST
PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
PPBUS_FW_FWBOOST
PP10V_FW
PP10V_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=10V
MAKE_BASE=TRUE
PP10V_FW
PP10V_FW
PPVP_FW
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=10V
MAKE_BASE=TRUE
PPVP_FW
PPVP_FW
PP3V3_FW_FWPHY
PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_FW_FWPHY
PP3V3_FW_FWPHY
PP1V0_FW
PP1V0_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V0_FW
PPVIN_FW_FWPHY
PPVIN_FW_FWPHY
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=10V
MAKE_BASE=TRUE
PPVIN_FW_FWPHY

"GPU" Rails

PP3V3_S0GPU
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_S0GPU
PP3V3_S0GPU
PP3V3_S0GPU
PP3V3_S0GPU
PP1V8_GPUIFPX
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_GPUIFPX
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS_R
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
PP1V8_S0GPU_ISNS_R
PP1V8_S0GPU_ISNS_R
PP1V05_S0GPU_ISNS_R
PP1V05_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0GPU_ISNS_R
PP1V05_S0GPU
PP1V05_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU
PPVCORE_GPU
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
PPVCORE_GPU

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE

Power Aliases

Apple Inc.

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Thermal Module Holes

ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH

Left CPU TM Hole
Right CPU TM Hole
Top GPU Right TM Hole
Bottom Left GPU TM Hole

Frame Holes

ZT0915 3R2P5 — GND
ZT0932 3R2P5
ZT0960 3R2P5
ZT0971 3R2P5
ZT0940 3R2P5
ZT0970 3R2P5

ZT0934 STDOFF-4.00D3.0H-SM
ZT0931 STDOFF-4.00D3.0H-SM
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
LCD_BKLT_EN — LCD_BKLT_EN
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PP3V3_S0 — PP3V3_S0
PM_ENET_EN — PM_ENET_EN
GND — GND
FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN
TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

GPU signals

PEG_D2R_P<15..0> — =PEG_D2R_P<0..15>
PEG_D2R_N<15..0> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<15..0> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<15..0> — =PEG_R2D_C_N<0..15>

** PEG LANES REVERSED. ARD STRAP REQ'D. **

R0902 3.0K 5% 1/10W MF-LF 402
CPU_CFG<3>

DP_IG_ML_P<3..0> — DP_IG_B_ML_P<3..0>
DP_IG_ML_N<3..0> — DP_IG_B_ML_N<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD
TP_SATA_EXTA_D2R_N — TP_SATA_EXTA_D2R_N
TP_SATA_EXTA_D2R_P — TP_SATA_EXTA_D2R_P
TP_SATA_EXTA_R2D_C_N — TP_SATA_EXTA_R2D_C_N
TP_SATA_EXTA_R2D_C_P — TP_SATA_EXTA_R2D_C_P

NC_GPU_XTALOUT — NC_GPU_XTALOUT
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>
TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM

USB Hub Aliases

EXCARD_OC_L — EXCARD_OC_L
USB_EXTC_OC_L — USB_EXTC_OC_L
USB_EXCARD_N — USB_EXCARD_N
USB_EXCARD_P — USB_EXCARD_P

Rev. A NCs

NC_ISNS_P1V05S0PCH_N — NC_ISNS_P1V05S0PCH_N
NC_ISNS_P1V05S0PCH_P — NC_ISNS_P1V05S0PCH_P
NC_ISNS_P3V3S0MPCH_N — NC_ISNS_P3V3S0MPCH_N
NC_ISNS_P3V3S0MPCH_P — NC_ISNS_P3V3S0MPCH_P
NC_ISNS_PVTTS0PCH_N — NC_ISNS_PVTTS0PCH_N
NC_ISNS_PVTTS0PCH_P — NC_ISNS_PVTTS0PCH_P

Per WF: R0914 can't be stuffed, it will break CPU IMON Calculation.
It will be removed from the design after protol.

PP1V8_S0GPU_ISNS
R0900 10 1% 1/10W MF-LF 402 — GPU_FB_A_VREF_DIV
R0901 10 1% 1/10W MF-LF 402 — GPU_FB_B_VREF_DIV

AUDIO ALIASES

PP5V_S0
XW0900 — PP5V_S0_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
XW0901 — PP5V_S0_AUDIO_AMP_R (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)
XW0902 — PP5V_S0_AUDIO_AMP_L (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V)

BKLT_PWR_PBUS
PPBUS_G3H
R0904 0 5% 1/10W MF-LF 603 — PPVIN_S0_LCDBKLT (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
R0903 0 5% 1/10W MF-LF 603 — PPVIN_S0_LCDBKLT
PP10V_FW
BKLT_PWR_FW10V

GMUX_VSYNC
BKL_SYNC
R0906 0 5% 1/16W MF-LF 402 — GMUX_VSYNC
R0907 0 5% 1/16W MF-LF 402 — LVDS_CONN_BKL_SYNC
PANEL_VSYNC

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

PAGE TITLE: Signal Aliases

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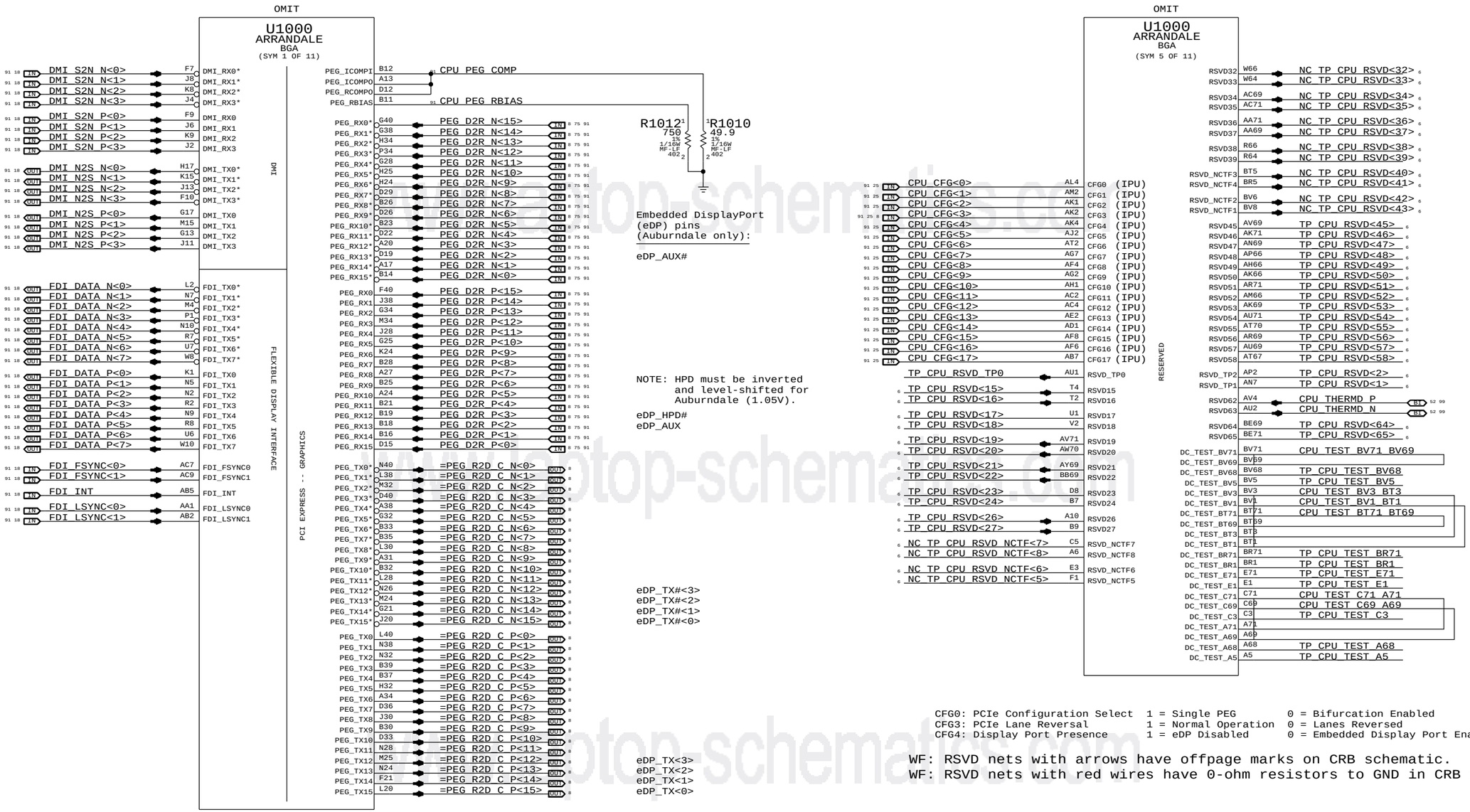

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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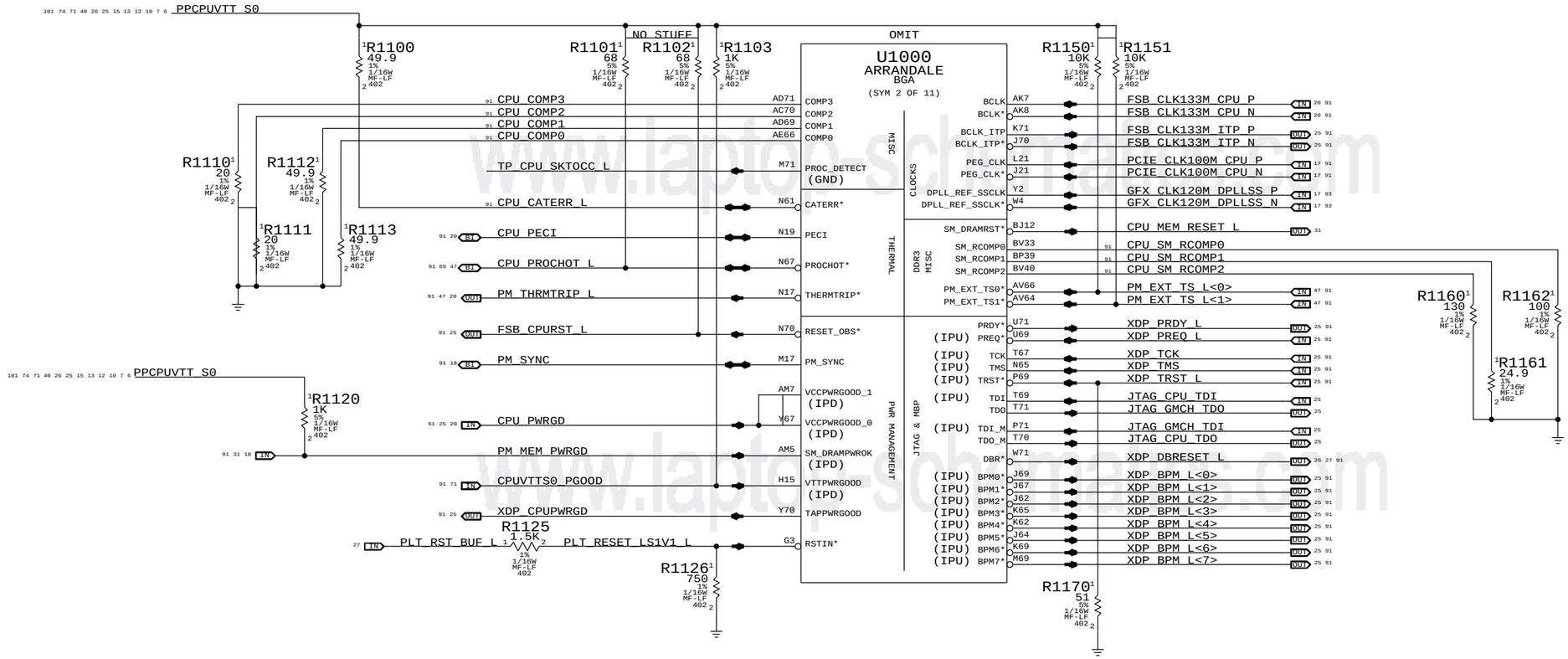

SYNC_MASTER=K18_MLB SYNC_DATE=10/14/2009

PAGE TITLE
CPU Clock/Misc/JTAG

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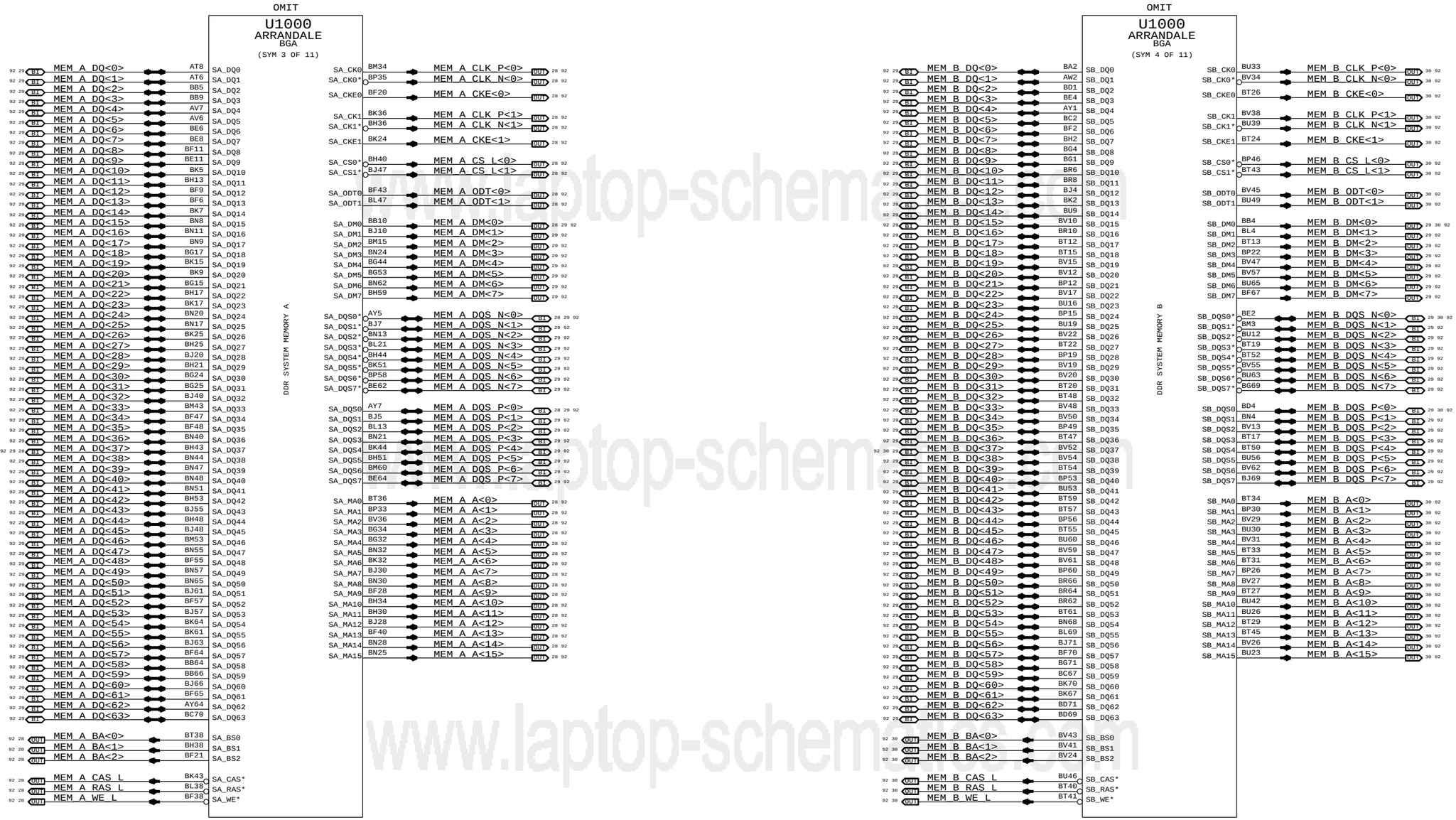

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PAGE TITLE

CPU DDR3 Interfaces

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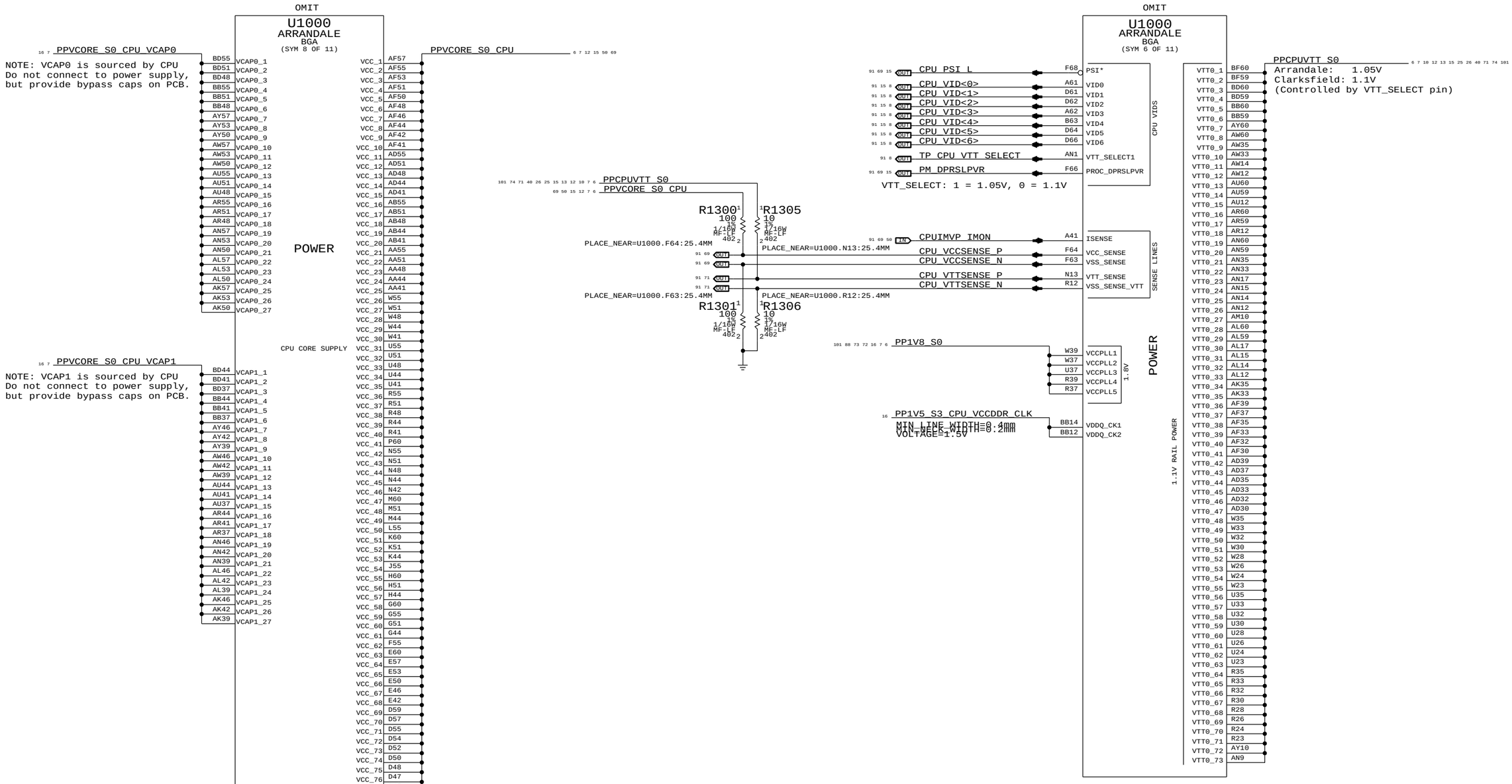
OMIT
U1000
ARRANDALE
BGA
(SYM 8 OF 11)
PPVCORE_S0_CPU_VCAP0
NOTE: VCAP0 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.
BD55 VCAP0_1
BD51 VCAP0_2
BD48 VCAP0_3
BB55 VCAP0_4
BB51 VCAP0_5
BB48 VCAP0_6
AY57 VCAP0_7
AY53 VCAP0_8
AY50 VCAP0_9
AW57 VCAP0_10
AW53 VCAP0_11
AW50 VCAP0_12
AU55 VCAP0_13
AU51 VCAP0_14
AU48 VCAP0_15
AR55 VCAP0_16
AR51 VCAP0_17
AR48 VCAP0_18
AN57 VCAP0_19
AN53 VCAP0_20
AN50 VCAP0_21
AL57 VCAP0_22
AL53 VCAP0_23
AL50 VCAP0_24
AK57 VCAP0_25
AK53 VCAP0_26
AK50 VCAP0_27
PPVCORE_S0_CPU_VCAP1
NOTE: VCAP1 is sourced by CPU
Do not connect to power supply,
but provide bypass caps on PCB.
BD44 VCAP1_1
BD41 VCAP1_2
BD37 VCAP1_3
BB44 VCAP1_4
BB41 VCAP1_5
BB37 VCAP1_6
AY46 VCAP1_7
AY42 VCAP1_8
AY39 VCAP1_9
AW46 VCAP1_10
AW42 VCAP1_11
AW39 VCAP1_12
AU44 VCAP1_13
AU41 VCAP1_14
AU37 VCAP1_15
AR44 VCAP1_16
AR41 VCAP1_17
AR37 VCAP1_18
AN46 VCAP1_19
AN42 VCAP1_20
AN39 VCAP1_21
AL46 VCAP1_22
AL42 VCAP1_23
AL39 VCAP1_24
AK46 VCAP1_25
AK42 VCAP1_26
AK39 VCAP1_27
POWER
CPU CORE SUPPLY
VCC_1 AF57
VCC_2 AF55
VCC_3 AF53
VCC_4 AF51
VCC_5 AF50
VCC_6 AF48
VCC_7 AF46
VCC_8 AF44
VCC_9 AF42
VCC_10 AF41
VCC_11 AD55
VCC_12 AD51
VCC_13 AD48
VCC_14 AD44
VCC_15 AD41
VCC_16 AB55
VCC_17 AB51
VCC_18 AB48
VCC_19 AB44
VCC_20 AB41
VCC_21 AA55
VCC_22 AA51
VCC_23 AA48
VCC_24 AA44
VCC_25 AA41
VCC_26 W55
VCC_27 W51
VCC_28 W48
VCC_29 W44
VCC_30 W41
VCC_31 U55
VCC_32 U51
VCC_33 U48
VCC_34 U44
VCC_35 U41
VCC_36 R55
VCC_37 R51
VCC_38 R48
VCC_39 R44
VCC_40 R41
VCC_41 P60
VCC_42 N55
VCC_43 N51
VCC_44 N48
VCC_45 N44
VCC_46 N42
VCC_47 M60
VCC_48 M51
VCC_49 M44
VCC_50 L55
VCC_51 K60
VCC_52 K51
VCC_53 K44
VCC_54 J55
VCC_55 H60
VCC_56 H51
VCC_57 H44
VCC_58 G60
VCC_59 G55
VCC_60 G51
VCC_61 G44
VCC_62 F55
VCC_63 E60
VCC_64 E57
VCC_65 E53
VCC_66 E50
VCC_67 E46
VCC_68 E42
VCC_69 D59
VCC_70 D57
VCC_71 D55
VCC_72 D54
VCC_73 D52
VCC_74 D50
VCC_75 D48
VCC_76 D47
VCC_77 D45
VCC_78 D43
VCC_79 B60
VCC_80 B56
VCC_81 B53
VCC_82 B49
VCC_83 B46
VCC_84 B42
VCC_85 A57
VCC_86 A54
VCC_87 A50
VCC_88 A47
VCC_89 A43
PPVCORE_S0_CPU
PPCPUVTT_S0
PPVCORE_S0_CPU
R1300 100 1% 1/16W MF-LF 402
R1305 10 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.F64:25.4MM
PLACE_NEAR=U1000.N13:25.4MM
PLACE_NEAR=U1000.F63:25.4MM
PLACE_NEAR=U1000.R12:25.4MM
R1301 100 1% 1/16W MF-LF 402
R1306 10 1% 1/16W MF-LF 402
OMIT
U1000
ARRANDALE
BGA
(SYM 6 OF 11)
CPU_PSI_L
CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
TP_CPU_VTT_SELECT
PM_DPRSLPVR
VTT_SELECT: 1 = 1.05V, 0 = 1.1V
F68 PSI*
A61 VID0
D61 VID1
D62 VID2
A62 VID3
B63 VID4
D64 VID5
D66 VID6
AN1 VTT_SELECT1
F66 PROC_DPRSLPVR
CPU VIDS
CPUIMVP_IMON
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VTTSENSE_P
CPU_VTTSENSE_N
A41 ISENSE
F64 VCC_SENSE
F63 VSS_SENSE
N13 VTT_SENSE
R12 VSS_SENSE_VTT
SENSE LINES
PP1V8_S0
W39 VCCPLL1
W37 VCCPLL2
U37 VCCPLL3
R39 VCCPLL4
R37 VCCPLL5
1.8V
POWER
PP1V5_S3_CPU_VCCDDR_CLK
MIN_LINE_WIDTH=0.4mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
BB14 VDDQ_CK1
BB12 VDDQ_CK2
1.1V RAIL POWER
PPCPUVTT_S0
Arrandale: 1.05V
Clarksfield: 1.1V
(Controlled by VTT_SELECT pin)
VTT0_1 BF60
VTT0_2 BF59
VTT0_3 BD60
VTT0_4 BD59
VTT0_5 BB60
VTT0_6 BB59
VTT0_7 AY60
VTT0_8 AW60
VTT0_9 AW35
VTT0_10 AW33
VTT0_11 AW14
VTT0_12 AW12
VTT0_13 AU60
VTT0_14 AU59
VTT0_15 AU12
VTT0_16 AR60
VTT0_17 AR59
VTT0_18 AR12
VTT0_19 AN60
VTT0_20 AN59
VTT0_21 AN35
VTT0_22 AN33
VTT0_23 AN17
VTT0_24 AN15
VTT0_25 AN14
VTT0_26 AN12
VTT0_27 AM10
VTT0_28 AL60
VTT0_29 AL59
VTT0_30 AL17
VTT0_31 AL15
VTT0_32 AL14
VTT0_33 AL12
VTT0_34 AK35
VTT0_35 AK33
VTT0_36 AF39
VTT0_37 AF37
VTT0_38 AF35
VTT0_39 AF33
VTT0_40 AF32
VTT0_41 AF30
VTT0_42 AD39
VTT0_43 AD37
VTT0_44 AD35
VTT0_45 AD33
VTT0_46 AD32
VTT0_47 AD30
VTT0_48 W35
VTT0_49 W33
VTT0_50 W32
VTT0_51 W30
VTT0_52 W28
VTT0_53 W26
VTT0_54 W24
VTT0_55 W23
VTT0_56 U35
VTT0_57 U33
VTT0_58 U32
VTT0_59 U30
VTT0_60 U28
VTT0_61 U26
VTT0_62 U24
VTT0_63 U23
VTT0_64 R35
VTT0_65 R33
VTT0_66 R32
VTT0_67 R30
VTT0_68 R28
VTT0_69 R26
VTT0_70 R24
VTT0_71 R23
VTT0_72 AY10
VTT0_73 AN9
SYNC_MASTER=K17 WFERRY
SYNC_DATE=06/09/2009
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CPU Power (1 of 2)
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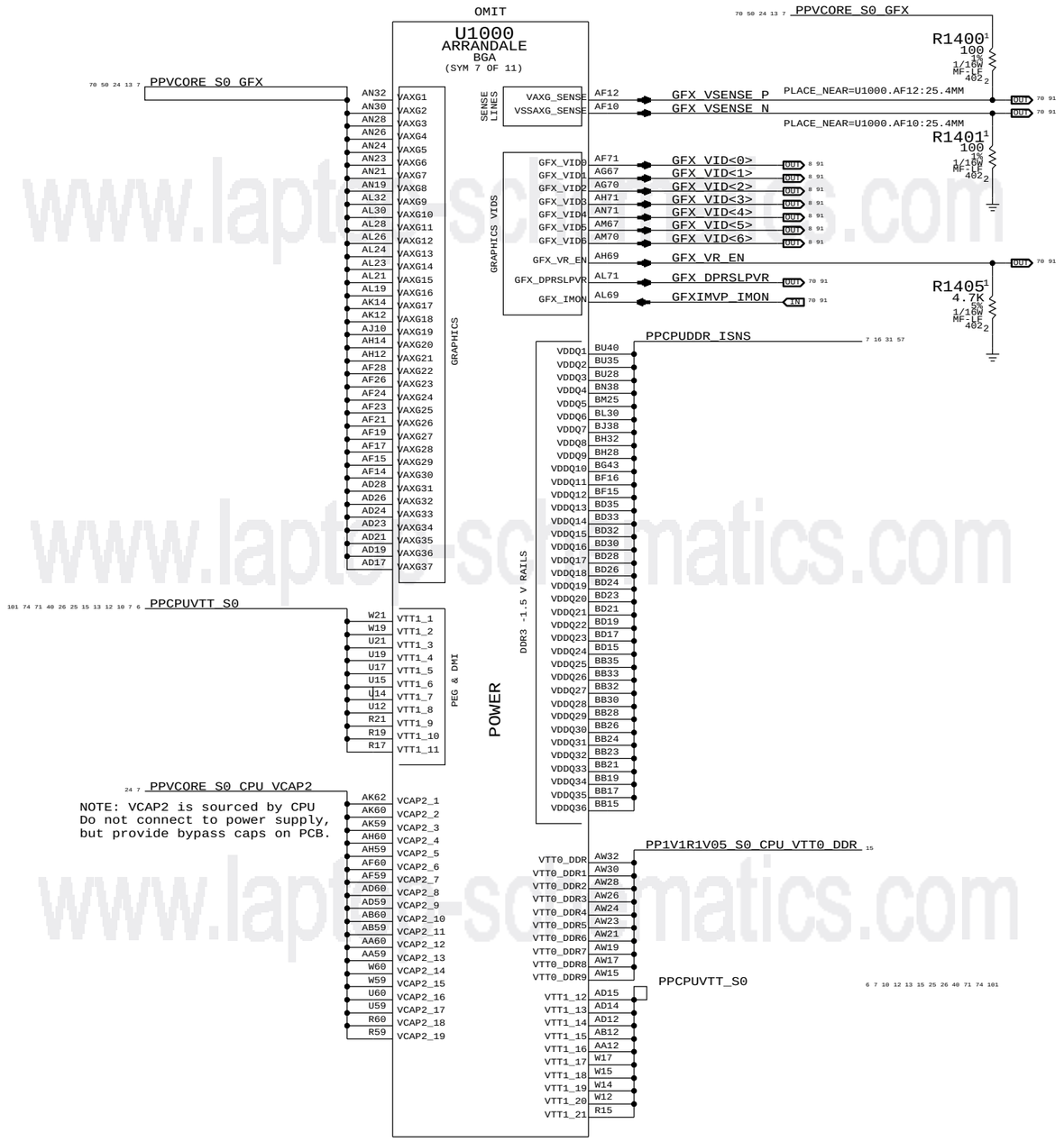

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BU62	VSS1	VSS76	AY62
BU58	VSS2	VSS77	AY59
BU55	VSS3	VSS78	AY55
BU51	VSS4	VSS79	AY51
BU48	VSS5	VSS80	AY48
BU44	VSS6	VSS81	AY44
BU37	VSS7	VSS82	AY41
BU32	VSS8	VSS83	AY37
BU25	VSS9	VSS84	AY35
BU21	VSS10	VSS85	AY33
BU18	VSS11	VSS86	AY32
BU14	VSS12	VSS87	AY30
BU11	VSS13	VSS88	AY28
BU7	VSS14	VSS89	AY26
BR42	VSS15	VSS90	AY24
BN64	VSS16	VSS91	AY23
BN6	VSS17	VSS92	AY21
BM70	VSS18	VSS93	AY19
BM51	VSS19	VSS94	AY17
BM44	VSS20	VSS95	AY15
BM32	VSS21	VSS96	AY14
BM24	VSS22	VSS97	AY12
BM17	VSS23	VSS98	AY8
BL57	VSS24	VSS99	AY4
BL55	VSS25	VSS100	AW67
BL48	VSS26	VSS101	AW62
BL40	VSS27	VSS102	AW59
BL28	VSS28	VSS103	AW55
BL20	VSS29	VSS104	AW51
BK63	VSS30	VSS105	AW48
BK60	VSS31	VSS106	AW44
BK53	VSS32	VSS107	AW41
BK34	VSS33	VSS108	AW37
BK10	VSS34	VSS109	AV9
BJ64	VSS35	VSS110	AV1
BJ21	VSS36	VSS111	AU70
BJ9	VSS37	VSS112	AU62
BJ1	VSS38	VSS113	AU57
BH70	VSS39	VSS114	AU53
BH57	VSS40	VSS115	AU50
BH55	VSS41	VSS116	AU46
BH47	VSS42	VSS117	AU42
BH24	VSS43	VSS118	AU39
BH20	VSS44	VSS119	AU35
BH15	VSS45	VSS120	AU33
BG51	VSS46	VSS121	AU32
BG36	VSS47	VSS122	AU30
BF62	VSS48	VSS123	AU28
BF30	VSS49	VSS124	AU26
BF13	VSS50	VSS125	AU24
BF8	VSS51	VSS126	AU23
BE70	VSS52	VSS127	AU21
BE65	VSS53	VSS128	AU19
BE9	VSS54	VSS129	AU17
BE1	VSS55	VSS130	AU15
BD57	VSS56	VSS131	AU14
BD53	VSS57	VSS132	AU4
BD50	VSS58	VSS133	AT64
BD46	VSS59	VSS134	AT10
BD42	VSS60	VSS135	AR62
BD39	VSS61	VSS136	AR57
BD14	VSS62	VSS137	AR53
BB71	VSS63	VSS138	AR50
BB62	VSS64	VSS139	AR46
BB57	VSS65	VSS140	AR42
BB53	VSS66	VSS141	AR39
BB50	VSS67	VSS142	AR35
BB46	VSS68	VSS143	AR33
BB42	VSS69	VSS144	AR32
BB39	VSS70	VSS145	AR30
BB7	VSS71	VSS146	AR28
BB1	VSS72	VSS147	AR26
BA70	VSS73	VSS148	AR24
AY71	VSS74	VSS149	AR23
AY66	VSS75	VSS150	AR21

OMIT

U1000
ARRANDALE
BGA
(SYM 10 OF 11)

AR19	VSS151	VSS226	BN71
AR17	VSS152	VSS227	E68
AR15	VSS153	VSS228	AH28
AR14	VSS154	VSS229	AH41
AR4	VSS155	VSS230	A66
AR1	VSS156	VSS231	AH26
AP70	VSS157	VSS232	BN1
AP64	VSS158	VSS233	A64
AN62	VSS159	VSS234	AH24
AN55	VSS160	VSS235	AH39
AN51	VSS161	VSS236	E5
AN48	VSS162	VSS237	AH23
AN44	VSS163	VSS238	C68
AN41	VSS164	VSS239	AH21
AN37	VSS165	VSS240	AH19
AN5	VSS166	VSS241	AH17
AN4	VSS167	VSS242	AH15
AM64	VSS168	VSS243	AH4
AM8	VSS169	VSS244	AG64
AL62	VSS170	VSS245	AG9
AL55	VSS171	VSS246	AG5
AL51	VSS172	VSS247	AF69
AL48	VSS173	VSS248	AF62
AL44	VSS174	VSS249	AF1
AL41	VSS175	VSS250	AE70
AL37	VSS176	VSS251	AE64
AL35	VSS177	VSS252	AD62
AL33	VSS178	VSS253	AD57
AL1	VSS179	VSS254	AD53
AK70	VSS180	VSS255	AD50
AK64	VSS181	VSS256	AD46
AK55	VSS182	VSS257	AD42
AK51	VSS183	VSS258	AD4
AK48	VSS184	VSS259	AC67
AK44	VSS185	VSS260	AC64
AK41	VSS186	VSS261	AC10
AK37	VSS187	VSS262	AC5
AK32	VSS188	VSS263	AC1
AK30	VSS189	VSS264	AB70
AK28	VSS190	VSS265	AB62
AK26	VSS191	VSS266	AB57
AK24	VSS192	VSS267	AB53
AK23	VSS193	VSS268	AB50
AK21	VSS194	VSS269	AB46
AK19	VSS195	VSS270	AB42
AK17	VSS196	VSS271	AB39
AK15	VSS197	VSS272	AB37
AJ70	VSS198	VSS273	AB35
AH62	VSS199	VSS274	AB33
AH57	VSS200	VSS275	AB32
AH55	VSS201	VSS276	AB30
AH53	VSS202	VSS277	AB28
BV66	VSS203	VSS278	AB26
AH51	VSS204	VSS279	AB24
BV64	VSS205	VSS280	AB23
AH50	VSS206	VSS281	AB21
BT68	VSS207	VSS282	AB19
AH48	VSS208	VSS283	AB17
BR69	VSS209	VSS284	AB15
BL71	VSS210	VSS285	AB14
AH46	VSS211	VSS286	AB9
BL1	VSS212	VSS287	AA66
AH37	VSS213	VSS288	AA64
BR68	VSS214	VSS289	AA62
R14	VSS215	VSS290	AA57
AH35	VSS216	VSS291	AA53
AH44	VSS217	VSS292	AA50
H71	VSS218	VSS293	AA46
AH33	VSS219	VSS294	AA42
BR3	VSS220	VSS295	AA39
F71	VSS221	VSS296	AA37
AH32	VSS222	VSS297	AA35
AH42	VSS223	VSS298	AA33
E69	VSS224	VSS299	AA32
AH30	VSS225	VSS300	AA30

OMIT

U1000
ARRANDALE
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AA28	VSS301	VSS367	K6
AA26	VSS302	VSS368	K4
AA24	VSS303	VSS369	J65
AA23	VSS304	VSS370	J57
AA21	VSS305	VSS371	J48
AA19	VSS306	VSS372	J47
AA17	VSS307	VSS373	J40
AA15	VSS308	VSS374	J9
AA14	VSS309	VSS375	H53
AA4	VSS310	VSS376	H43
W69	VSS311	VSS377	H36
W62	VSS312	VSS378	H1
W57	VSS313	VSS379	G70
W53	VSS314	VSS380	G57
W50	VSS315	VSS381	G53
W46	VSS316	VSS382	G48
W42	VSS317	VSS383	G47
W6	VSS318	VSS384	G43
W1	VSS319	VSS385	G30
V70	VSS320	VSS386	G24
U64	VSS321	VSS387	G20
U62	VSS322	VSS388	G15
U57	VSS323	VSS389	F61
U53	VSS324	VSS390	F48
U50	VSS325	VSS391	F47
U46	VSS326	VSS392	F28
U42	VSS327	VSS393	F20
U39	VSS328	VSS394	F4
U9	VSS329	VSS395	E37
U4	VSS330	VSS396	E33
T1	VSS331	VSS397	E30
R70	VSS332	VSS398	E16
R62	VSS333	VSS399	E12
R57	VSS334	VSS400	D41
R53	VSS335	VSS401	D38
R50	VSS336	VSS402	D34
R46	VSS337	VSS403	D31
R42	VSS338	VSS404	D27
R5	VSS339	VSS405	D24
P4	VSS340	VSS406	D20
N63	VSS341	VSS407	D17
N57	VSS342	VSS408	D13
N53	VSS343	VSS409	D10
N50	VSS344	VSS410	D6
N46	VSS345	VSS411	B65
N30	VSS346	VSS412	B62
N21	VSS347	VSS413	B58
N15	VSS348	VSS414	B55
N53	VSS349	VSS415	B51
M42	VSS350	VSS416	B48
M36	VSS351	VSS417	B44
M1	VSS352	VSS418	A59
L70	VSS353	VSS419	A55
L57	VSS354	VSS420	A52
L48	VSS355	VSS421	A48
L47	VSS356	VSS422	A45
L13	VSS357	VSS423	A40
K64	VSS358	VSS424	A36
K53	VSS359	VSS425	A33
K43	VSS360	VSS426	A29
K36	VSS361	VSS427	A26
K34	VSS362	VSS428	A22
K32	VSS363	VSS429	A19
K25	VSS364	VSS430	A15
K17	VSS365	VSS431	A12
K11	VSS366	VSS432	A8
		VSS433	B40

SYNC_MASTER=K17_REF SYNC_DATE=04/29/2009

PAGE TITLE

CPU Grounds

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CPU VCore HF and Bulk Decoupling

3x 470uF 4.5mOhm, 1x 330uF, 15x 22uF 0603, 25x 1uF 0402

69 50 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
1UF 10% 16V X5R 402

C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 16V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1626 C1627 NO STUFF C1628 C1629 NO STUFF C1630 NO STUFF C1631 NO STUFF C1632 C1633 C1634 C1691 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 C1637 C1638 NO STUFF C1639 C1640 NO STUFF C1641 C1643 C1644 C1645 NO STUFF C1646 C1647 NO STUFF C1648 C1699
22UF 20% 6.3V X5R-CERM 603

C1649 330UF 20% 2.0V POLY-TANT D2T-SM2
C1650 C1651 C1652 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NO STUFF C16A0 C16A1 C16A2 C16A3 C16A4 62UF 20% 11V ELEC CASE-B2

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

15 13 12 10 7 6 PPCPUVTT_S0

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
1UF 10% 10V X5R 402

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 10V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

101 74 71 40 26 25 15 13 12 10 7 6 PPCPUVTT_S0

R1600 R1602 CPUPOC4U R1604 NO STUFF R1606 NO STUFF R1608
1K 5% 1/16W MF-LF 402

CPUPOC3U R1601 CPUPOC3U R1603 CPUPOC5U R1605 R1607

91 12 8 CPU_VID<0>
91 12 8 CPU_VID<1>
91 12 8 CPU_VID<2>
91 12 8 CPU_VID<3>
91 12 8 CPU_VID<4>
91 12 8 CPU_VID<5>
91 12 8 CPU_VID<6>
91 69 12 PM_DPRSLPVR
91 69 12 CPU_PSI_L

NO STUFF R1610 NO STUFF R1612 CPUPOC4D R1614 R1616 R1618
1K 5% 1/16W MF-LF 402

NO STUFF R1611 CPUPOC3D R1613 CPUPOC5D R1615 NO STUFF R1617

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly. Instead call out appropriate BOM GROUP defined in tables above.

VTT0_DDR DECOUPLING

3x 1uF 0402

L1695 30-OHM-5A 0603

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

PP1V1R1V05_S0_CPU_VTT0_DDR 13
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

C1695 C1696 C1697
1UF 10% 10V X5R 402

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU Non-GFX Decoupling (1 of 2)

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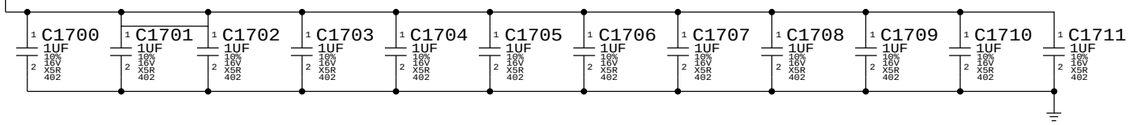
VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP0



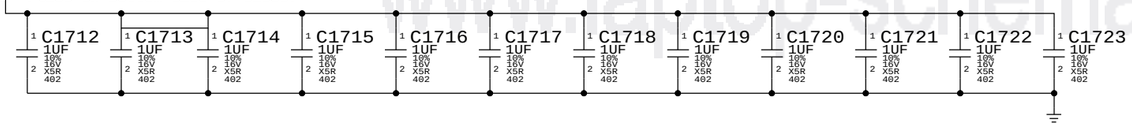
VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

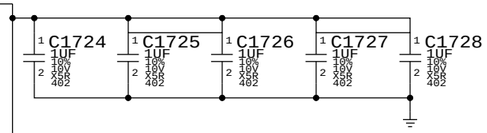
12 7 PPVCORE_S0_CPU_VCAP1



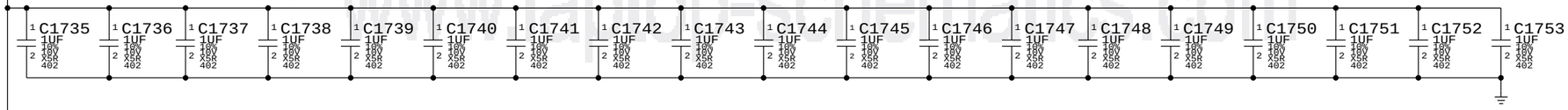
Memory (CPU VCCDDR) DECOUPLING

5x 1uF 0402

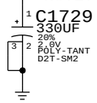
57 31 16 13 7 PPCPUDDR_ISNS



NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.



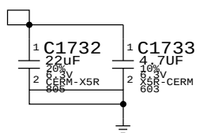
NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. 2x330uF on CSA73. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

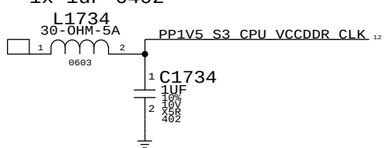
88 73 72 12 7 6 101 PP1V8_S0



DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

57 31 16 13 7 PPCPUDDR_ISNS



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F
actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC_MASTER=K17_REF SYNC_DATE=06/24/2009

PAGE TITLE: CPU Non-GFX Decoupling (2 of 2)

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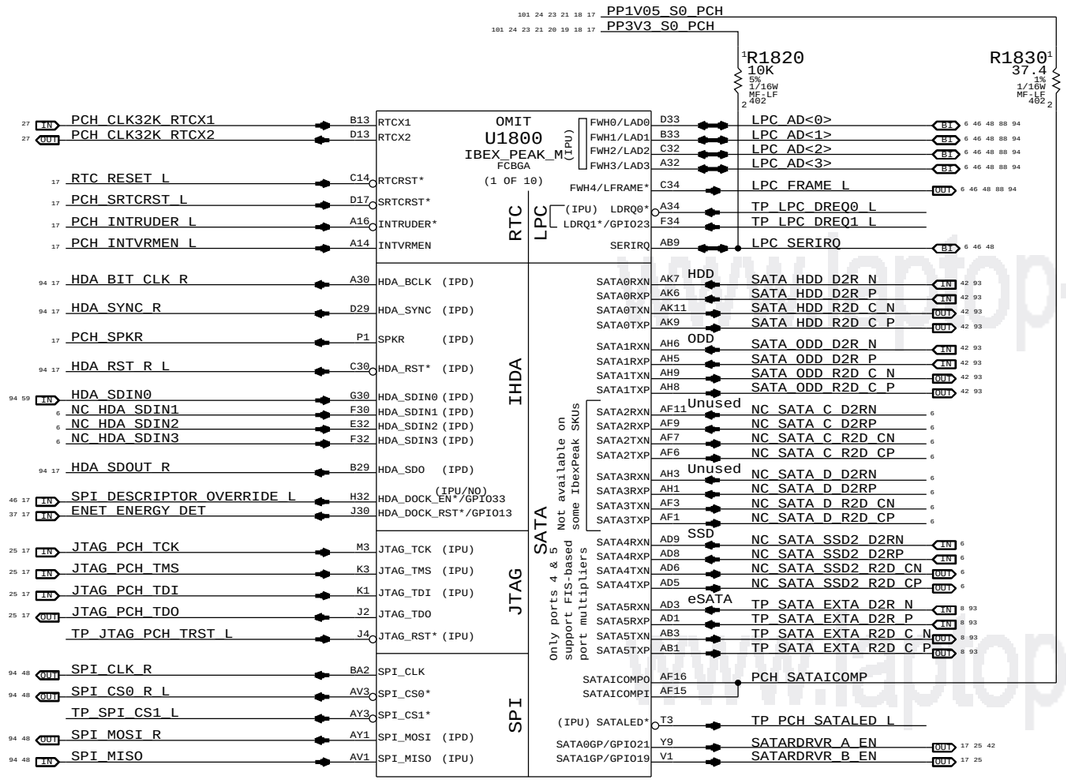

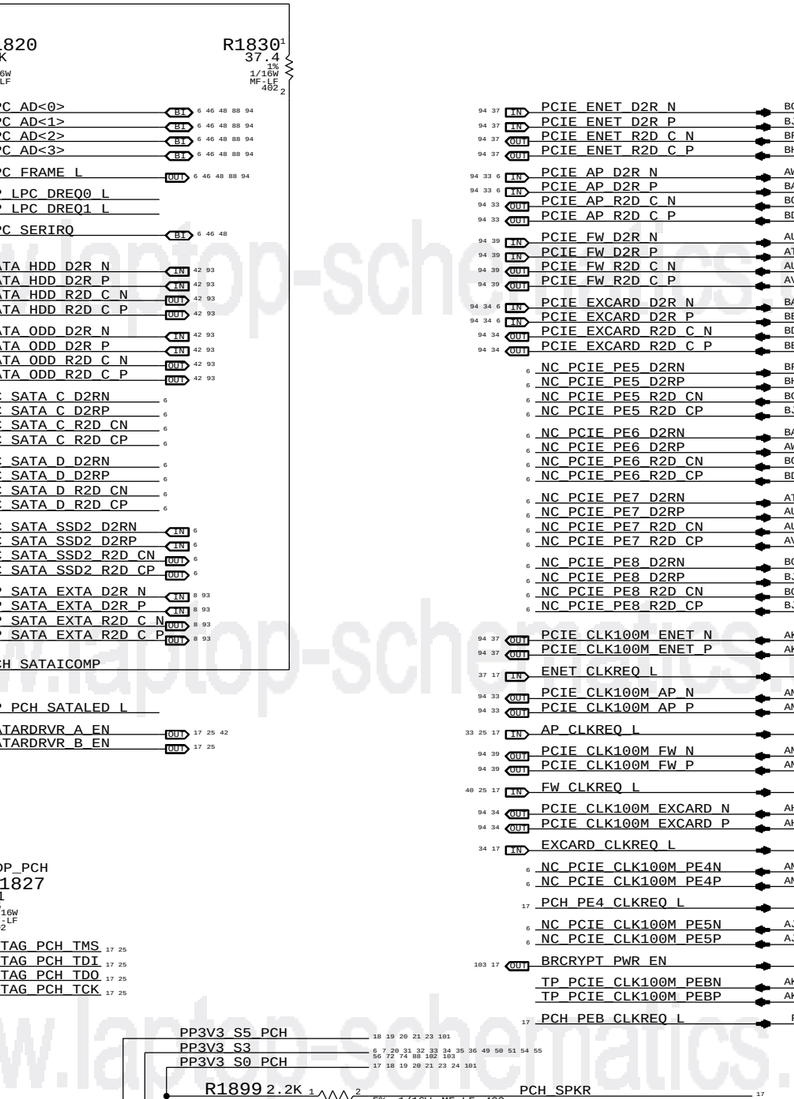

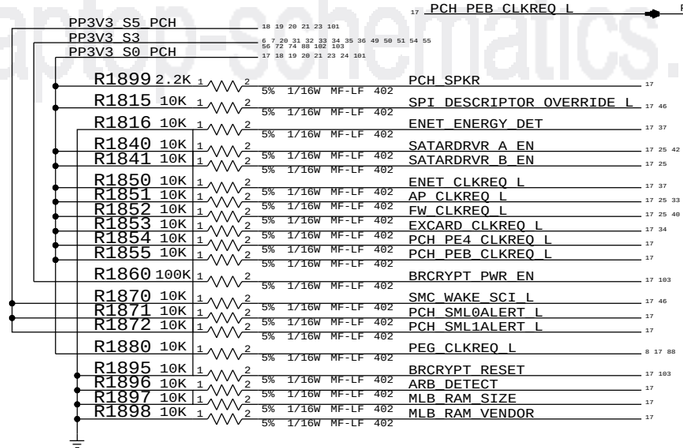

SYNC_MASTER=K17_REF SYNC_DATE=08/24/2009

PAGE TITLE

PCH SATA/PCIE/CLK/LPC/SPI

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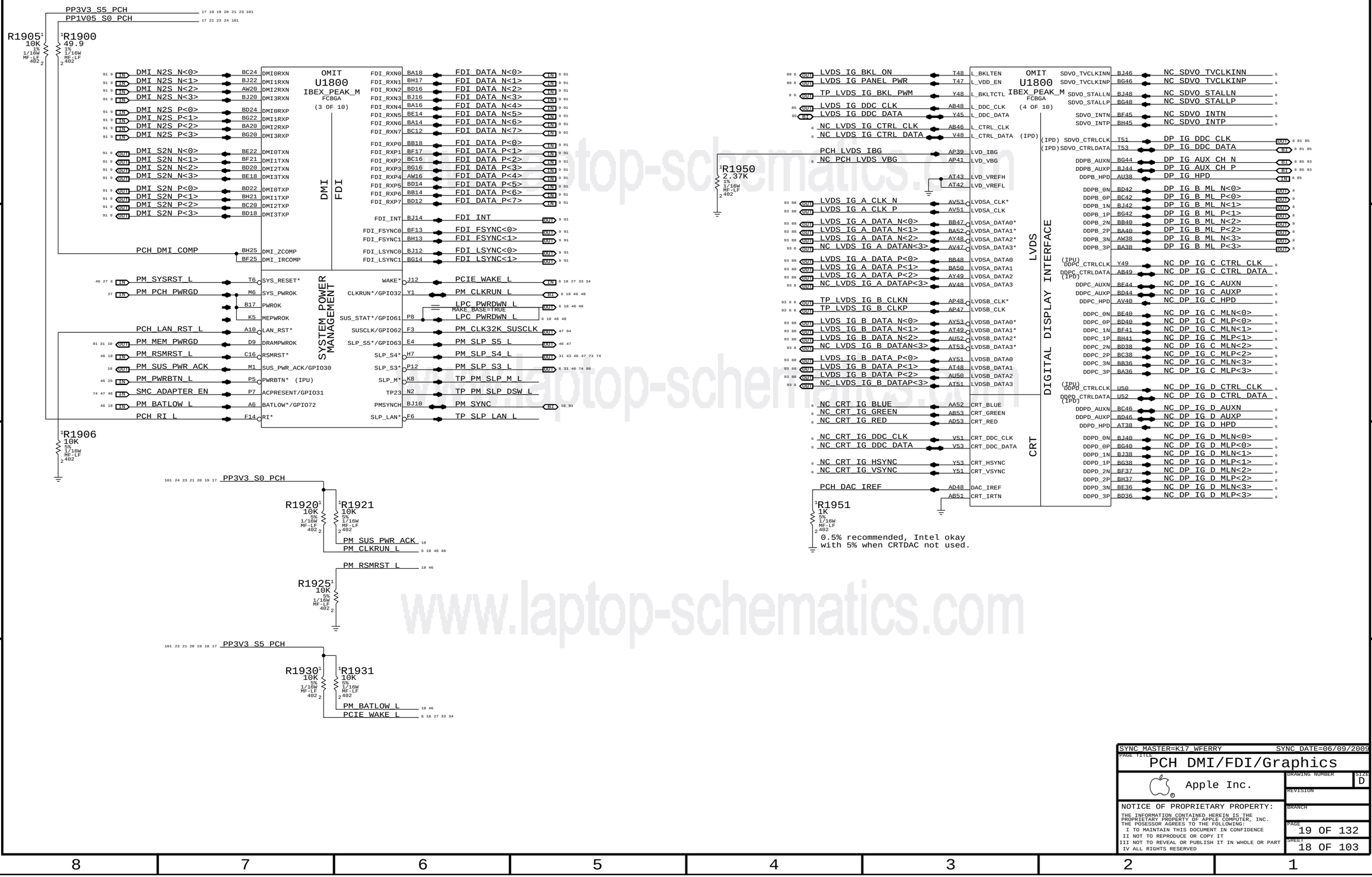

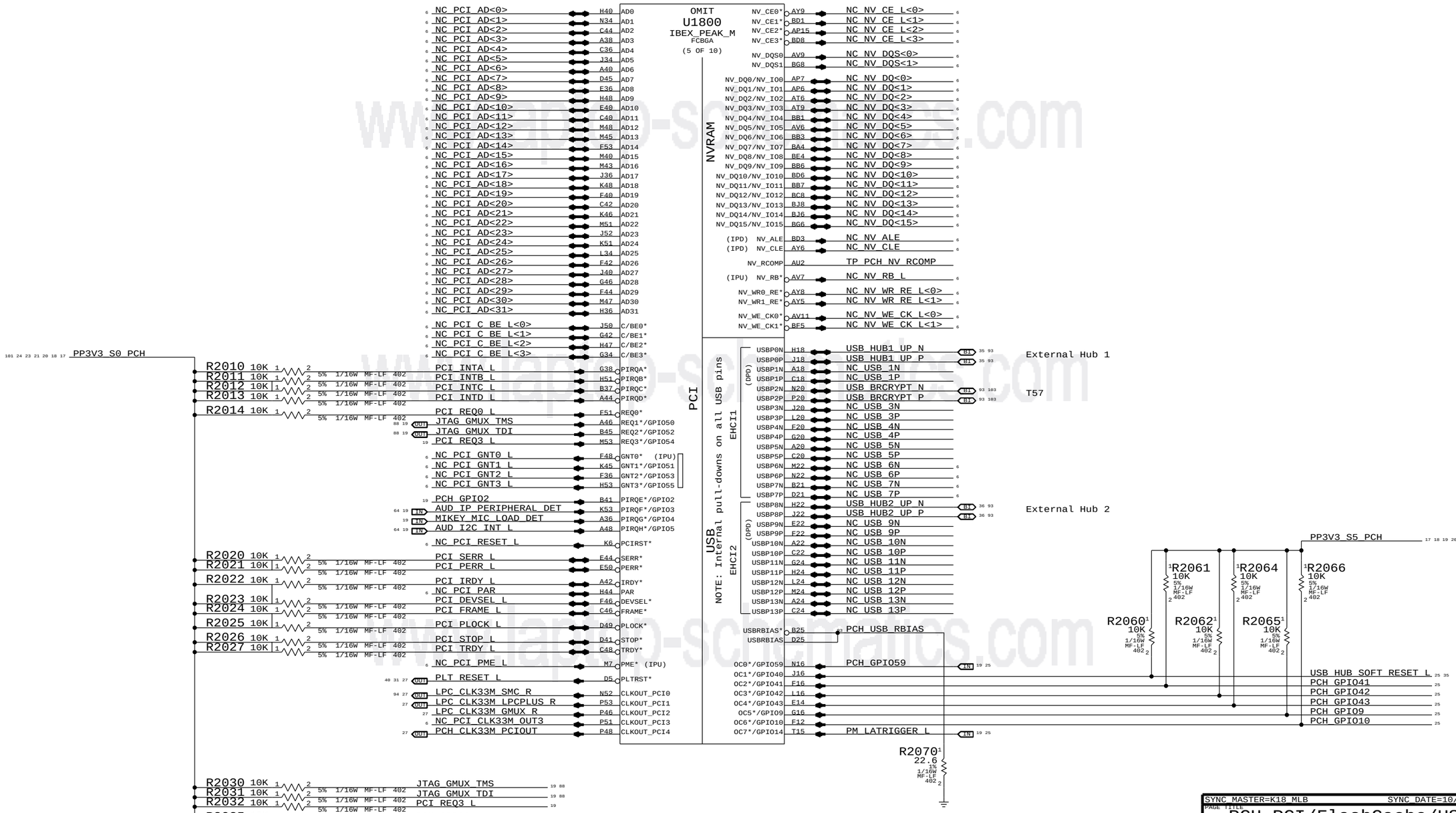

SYNC_MASTER=K18_MLB	SYNC_DATE=10/07/2009
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IPU* = Only on TACH function.

47 46 25 20 IN	SMC_IG_THROTTLE_L	Y3	BMBUSY*/GPIO0			
40 20 8 IN	FW_PLUG_DET_L	C38	TACH1/GPIO1 (IPU*)			
88 20 IN	GMUX_INT	D37	TACH2/GPIO6 (IPU*)			
46 20 IN	SMC_RUNTIME_SCI_L	J32	TACH3/GPIO7 (IPU*)			
20	PCH_FCIM_EN_L	F10	GPIO8 (IPU)			
37 20 OUT	ENET_LOW_PWR	K9	LAN_PHY_PWR_CTRL/GPIO12			
20	PCH_GPIO15	T7	GPIO15 (IPD)			
64 25 20 OUT	AUD_IPHS_SWITCH_EN	AA2	SATA4GP/GPIO16			
48 20 6 BI	LPCPLUS_GPIO	F38	TACH0/GPIO17 (IPU*)			
42 20 OUT	ODD_PWR_EN_L	Y7	SCLOCK/GPIO22			
20	PCH_GPIO24	H10	MEM_LED/GPIO24			
20	PCH_VRM_EN	AB12	GPIO27			
31 25 OUT	ISOLATE_CPU_MEM_L	V13	GPIO28 (IPU)			
	TP_PCH_STP_PCI_L	M11	STP_PCI*/GPIO34			
20 OUT	MXM_GOOD	V6	SATACLKREQ*/GPIO35			
25 20 OUT	SDCARD_RESET	AB7	SATA2GP/GPIO36			
88 25 20 OUT	JTAG_GMUX_TCK	AB13	SATA3GP/GPIO37			
88 20 IN	JTAG_GMUX_TDO	V3	SLOAD/GPIO38			
20	PCH_GPIO39	P3	SDATAOUT0/GPIO39			
74 20 OUT	WOL_EN	H3	PCIECLKRQ6*/GPIO45			
74 33 20 OUT	AP_PWR_EN	F1	PCIECLKRQ7*/GPIO46			
40 20 OUT	FW_PWR_EN	AB6	SDATAOUT1/GPIO48			
25 20 OUT	ME_TEMP_ALERT_L	AA4	SATA5GP/GPIO49			
58 48 20 6 BI	SPIROM_USE_MLB	F8	GPIO57			

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U1800
IBEX_PEAK_M
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GPIO

94 6	PCH_VSS_NCTF<1>	A4	VSS_NCTF1			
94 6	PCH_VSS_NCTF<2>	A49	VSS_NCTF2			
		A5	VSS_NCTF3			
		A50	VSS_NCTF4			
94 6	PCH_VSS_NCTF<5>	A52	VSS_NCTF5			
		A53	VSS_NCTF6			
94	TP_PCH_VSS_NCTF<7>	B2	VSS_NCTF7			
		B4	VSS_NCTF8			
94 6	PCH_VSS_NCTF<9>	B52	VSS_NCTF9			
		B53	VSS_NCTF10			
94 6	PCH_VSS_NCTF<11>	BE1	VSS_NCTF11			
94 6	PCH_VSS_NCTF<12>	BE53	VSS_NCTF12			
		BF1	VSS_NCTF13			
		BF53	VSS_NCTF14			
94 6	PCH_VSS_NCTF<15>	BH1	VSS_NCTF15			
		BH2	VSS_NCTF16			
94 6	PCH_VSS_NCTF<17>	BH52	VSS_NCTF17			
		BH53	VSS_NCTF18			
94 6	PCH_VSS_NCTF<19>	BJ1	VSS_NCTF19			
		BJ2	VSS_NCTF20			
94 6	PCH_VSS_NCTF<21>	BJ4	VSS_NCTF21			
94	PCH_VSS_NCTF<22>	BJ49	VSS_NCTF22			
		BJ5	VSS_NCTF23			
		BJ50	VSS_NCTF24			
94 6	PCH_VSS_NCTF<25>	BJ52	VSS_NCTF25			
		BJ53	VSS_NCTF26			
94 6	PCH_VSS_NCTF<27>	D1	VSS_NCTF27			
		D2	VSS_NCTF28			
94 6	PCH_VSS_NCTF<29>	D53	VSS_NCTF29			
		E1	VSS_NCTF30			
		E53	VSS_NCTF31			

NCTF

RSVD

CPU

MISC

CLKOUT_PCIE6N	AH45	NC_PCIE_CLK100M_PE6N	6			
CLKOUT_PCIE6P	AH46	NC_PCIE_CLK100M_PE6P	6			
CLKOUT_PCIE7N	AF48	NC_PCIE_CLK100M_PE7N	6			
CLKOUT_PCIE7P	AF47	NC_PCIE_CLK100M_PE7P	6			
A20GATE	U2	PCH_A20GATE				
CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	FSB_CLK133M_CPU_N	OUT 10 91			
CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	FSB_CLK133M_CPU_P	OUT 10 91			
PECI	BG10	CPU_PECI	BI 10 91			
RCIN*	T1	PCH_RCIN_L				
PROCPWRGD	BE10	CPU_PWRGD	OUT 10 25 91			
THRMTRIP*	BD10	PCH_THRMTRIP_L				
TP1	BA22	NC_PCH_TP1	6			
TP2	AW22	NC_PCH_TP2	6			
TP3	BB22	NC_PCH_TP3	6			
TP4	AY45	NC_PCH_TP4	6	(DPL_B_MON1_N)		
TP5	AY46	NC_PCH_TP5	6	(DPL_B_MON1_P)		
TP6	AV43	NC_PCH_TP6	6	(DPL_B_MON2_N)		
TP7	AV45	NC_PCH_TP7	6	(DPL_B_MON2_P)		
TP8	AF13	NC_PCH_TP8	6	(SATA_OB_ANA)		
TP9	M18	NC_PCH_TP9	6			
TP10	N18	NC_PCH_TP10	6			
TP11	AJ24	NC_PCH_TP11	6			
TP12	AK41	NC_PCH_TP12	6	(XCKPLL_MON1_N)		
TP13	AK42	NC_PCH_TP13	6	(XCKPLL_MON1_P)		
TP14	M32	NC_PCH_TP14	6			
TP15	N32	NC_PCH_TP15	6			
TP16	M30	NC_PCH_TP16	6			
TP17	N30	NC_PCH_TP17	6			
TP18	H12	NC_PCH_TP18	6			
TP19	AA23	NC_PCH_TP19	6			
NC_1	AB45	NC_PCH_NC1	6			
NC_2	AB38	NC_PCH_NC2	6			
NC_3	AB42	NC_PCH_NC3	6			
NC_4	AB41	NC_PCH_NC4	6			
NC_5	T39	NC_PCH_NC5	6			
(IPD) INIT3_3V*	P6	TP_PCH_INIT3V3_L				
TP24	C10	NC_PCH_SST	6			

PP3V3_S0_PCH 17 18 19 20 21 23 24 101

R2150 10K 5% 1/16W MF-LF 402 (1 to PP3V3_S0_PCH, 2 to RCIN*)

R2155 10K 5% 1/16W MF-LF 402 (1 to PP3V3_S0_PCH, 2 to THRMTRIP*)

PPVTT_S0_PCH 21 23 101

R2160 56 5% 1/16W MF-LF 402 (1 to PPVTT_S0_PCH, 2 to THRMTRIP*)

R2161 56 5% 1/16W MF-LF 402 (1 to THRMTRIP*, 2 to PM_THRMTRIP_L)

PM_THRMTRIP_L IN 10 47 91

PP3V3_S5_PCH 17 18 19 21 23 101
PP3V3_S3 6 7 17 31 32 33 34 35 36 49 50 51 54 55 56 72 74 88 102 103
PP3V3_S0_PCH 17 18 19 20 21 23 24 101

R2110	10K	SMC_IG_THROTTLE_L	20 25 46 47
R2111	10K	FW_PLUG_DET_L	8 20 40
R2112	20K	GMUX_INT	20 88
R2113	10K	SMC_RUNTIME_SCI_L	20 46
R2114	10K	PCH_FCIM_EN_L	20
R2115	2.2K	ENET_LOW_PWR	20 37
R2116	10K	PCH_GPIO15	20
R2120	10K	AUD_IPHS_SWITCH_EN	20 25 64
R2121	10K	LPCPLUS_GPIO	6 20 48
R2122	10K	ODD_PWR_EN_L	20 42
R2123	10K	PCH_GPIO24	20
R2124	10K	PCH_VRM_EN	20
R2130	10K	MXM_GOOD	20
R2131	10K	SDCARD_RESET	20 25
R2132	10K	JTAG_GMUX_TCK	20 25 88
R2133	10K	JTAG_GMUX_TDO	20 88
R2134	10K	PCH_GPIO39	20
R2135	10K	WOL_EN	20 74
R2136	10K	AP_PWR_EN	20 33 74
R2137	10K	FW_PWR_EN	20 40
R2138	10K	ME_TEMP_ALERT_L	20 25
R2139	100K	SPIROM_USE_MLB	6 20 48 58

All: 5% 1/16W MF-LF 402

SYNC_MASTER=K18_MLB SYNC_DATE=11/13/2009

PAGE TITLE: PCH MISC

Apple Inc.

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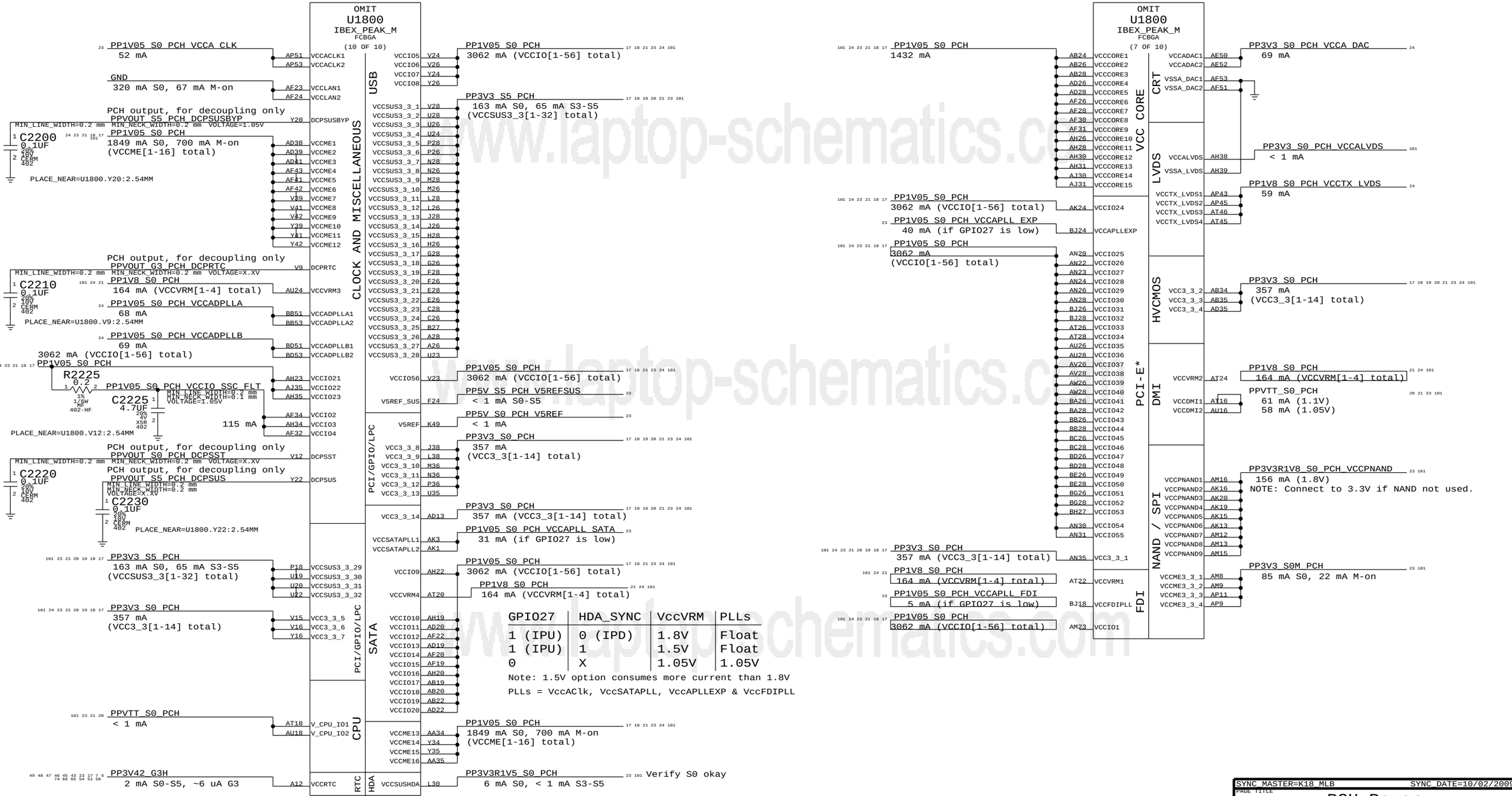

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K18_MLB SYNC_DATE=10/02/2009

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER | SIZE: D

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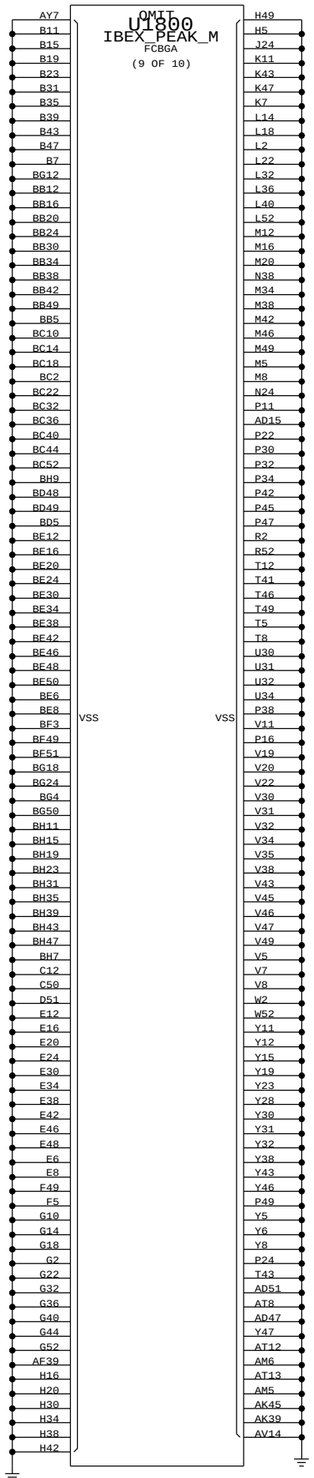

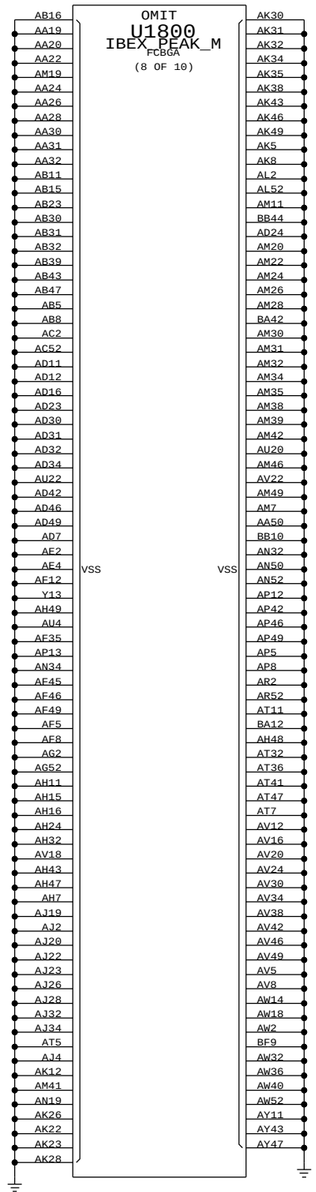

SYNC_MASTER=T22_MLB SYNC_DATE=03/26/2009

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER D

REVISION

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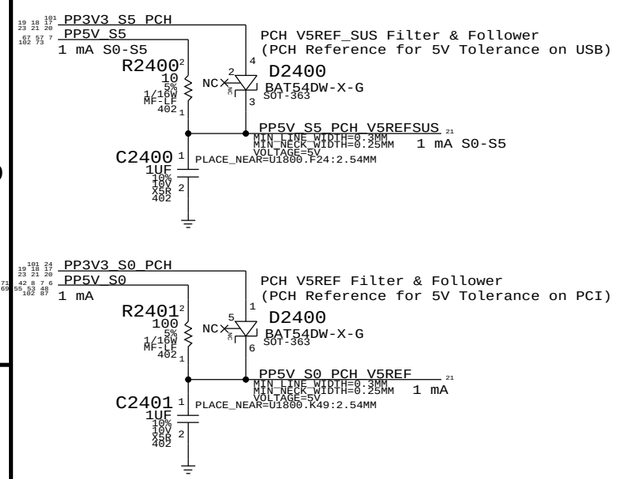

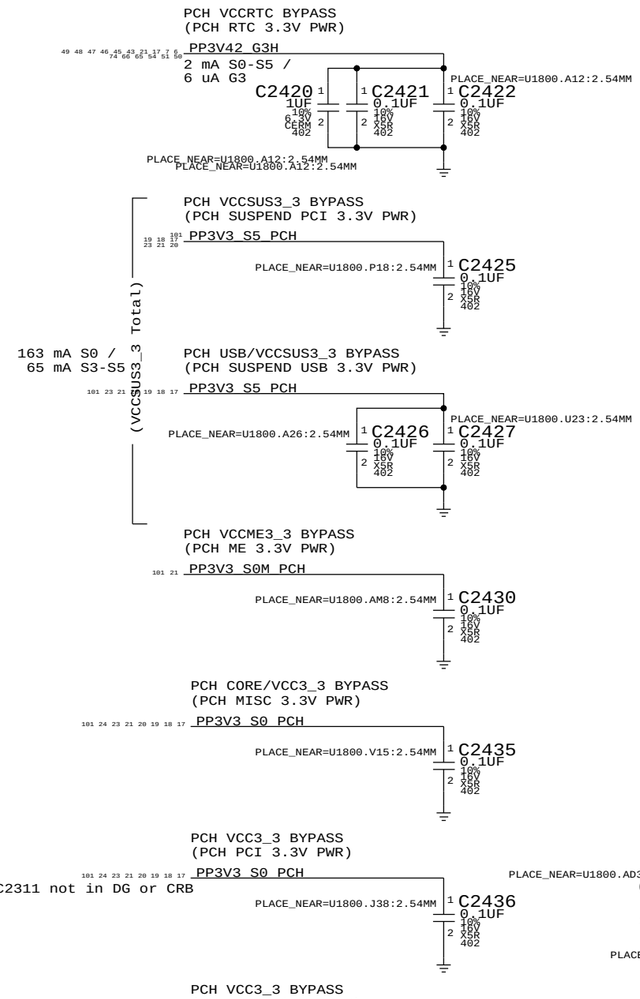

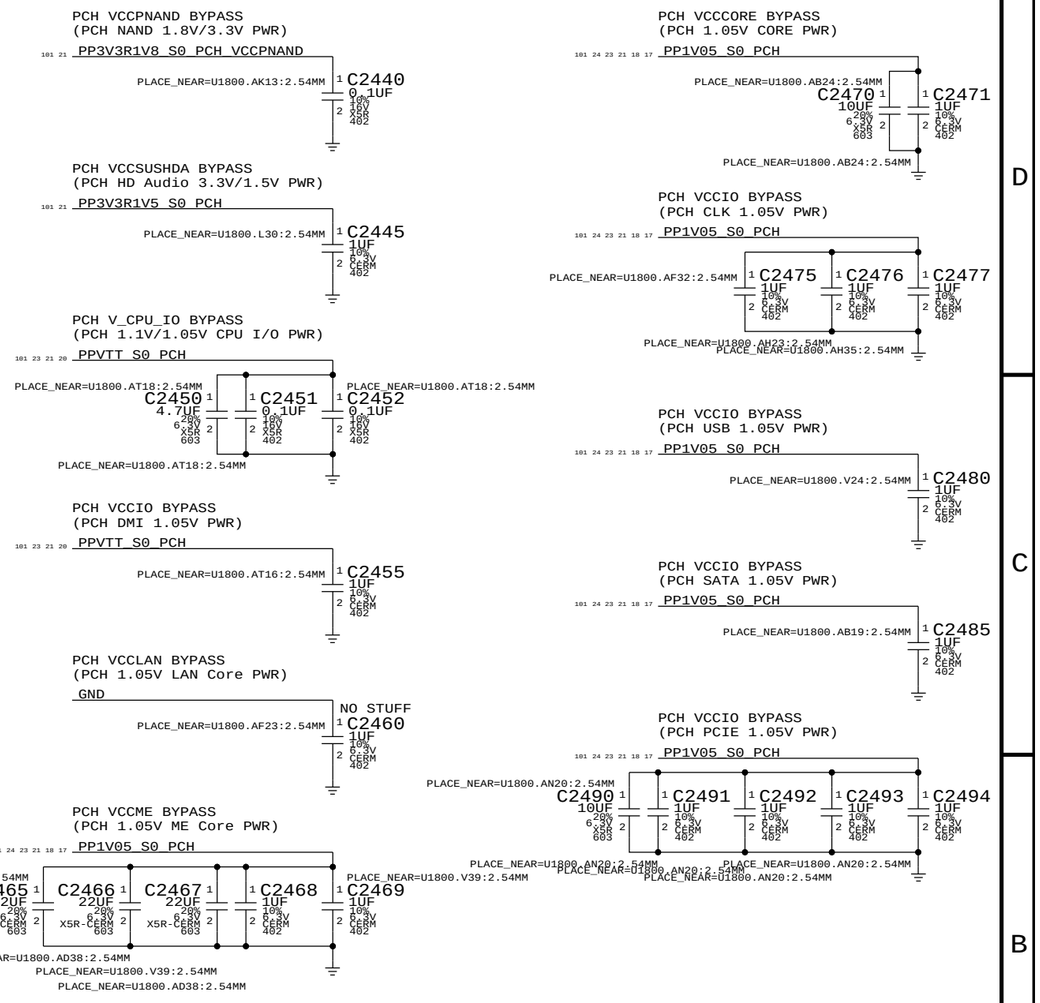

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE
PCH Non-GFX Decoupling

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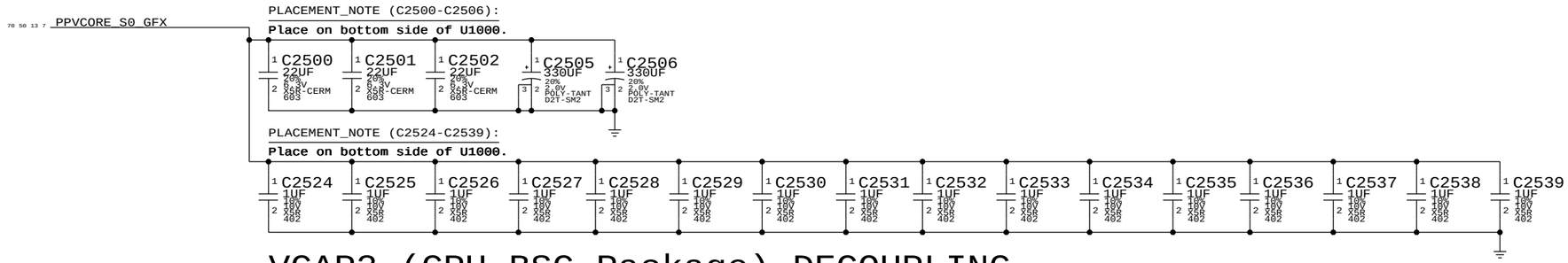
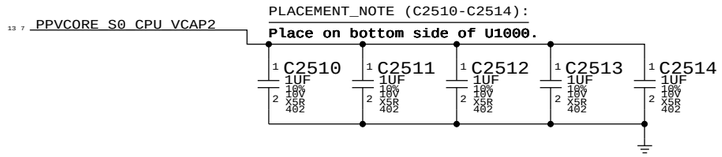
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

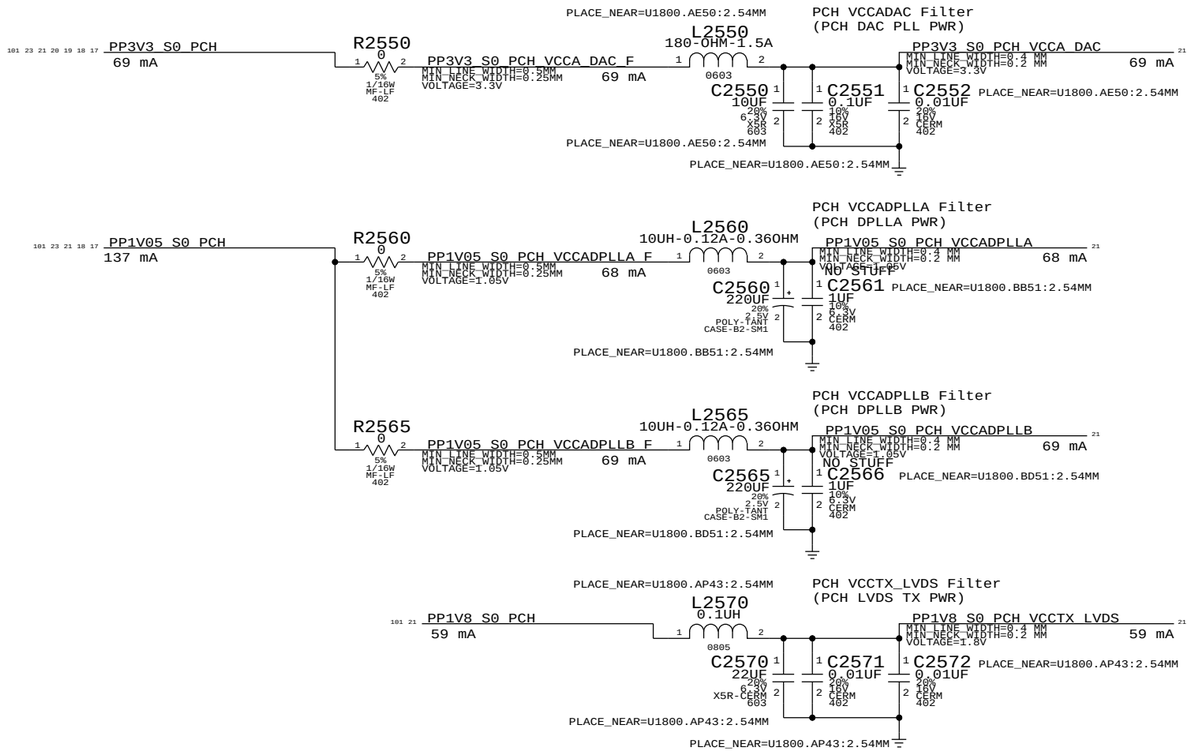


VCAP2 (CPU BSC Package) DECOUPLING

5x 1uF 0402



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE
CPU/PCH GFX Decoupling

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Calpella Processor mini XDP

PPCPUVTT_S0

CRITICAL
XDP_CONN
J2600
LTH-030-01-G-D-NOPEGS
F-ST-SM
998-1571

XDP_CPU_BPM
RP2600
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>

XDP_CPU_CFG
RP2601
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

PLACEMENT_NOTE=Place R2601 close to R2600 to minimize stubs.

XDP R2615 51 5% 1/16W MF-LF 402

XDP_PREQ_L
XDP_PRDY_L
XDP_OBSDATA_A<0>
XDP_OBSDATA_A<1>
XDP_OBSDATA_A<2>
XDP_OBSDATA_A<3>
CPU_CFG<17>
CPU_CFG<16>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>
XDP_PWRGD
PM_PWRBTN_L
XDP_CPUPWRGD
TP_XDP_HOOK3
SMBUS_PCH_DATA
SMBUS_PCH_CLK
XDP_TCK

OBSFN_A0 OBSFN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSFN_B0 OBSFN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSFN_C0 OBSFN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSFN_D0 OBSFN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<8> CPU_CFG<9> CPU_CFG<0> CPU_CFG<1> CPU_CFG<2> CPU_CFG<3> CPU_CFG<10> CPU_CFG<11> CPU_CFG<4> CPU_CFG<5> CPU_CFG<6> CPU_CFG<7> FSB_CLK133M_ITP_P FSB_CLK133M_ITP_N

XDP R2610 1K 5% 1/16W MF-LF 402
XDP R2611 1K 5% 1/16W MF-LF 402
FSB_CPURST_L
PLACE_NEAR=U1000.N70:1.00MM

XDP_CPURST_L
XDP_DBRESET_L
NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
XDP_TDO
XDP_TRST_L
XDP_TDI
XDP_TMS

XDP C2600 0.1uF 10% 16V X5R 402
XDP C2601 0.1uF 10% 16V X5R 402

XDP_NORMAL&XDP_CPU R2690 0 5% 1/16W MF-LF 402
XDP_CPU R2695 0 5% 1/16W MF-LF 402
XDP_NORMAL R2691 0 5% 1/16W MF-LF 402
XDP_GMCH R2696 0 5% 1/16W MF-LF 402
XDP_NORMAL&XDP_GMCH R2692 0 5% 1/16W MF-LF 402

JTAG_CPU_TDI → XDP_TDI
JTAG_CPU_TDO → XDP_TDO
JTAG_GMCH_TDI
JTAG_GMCH_TDO

Calpella PCH mini XDP

PP3V3_S0

NOTE: This is not the standard XDP pinout.
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT PCH DEBUGGING.

CRITICAL
XDP_CONN
J2650
DF40C-60DS-0.4V
F-ST-SM
998-2515

TP_XDPPCH_OBSFN_A<0>
TP_XDPPCH_OBSFN_A<1>
PCH_GPIO59
USB_HUB_SOFT_RESET_L
PCH_GPIO41
PCH_GPIO42
TP_XDPPCH_OBSFN_B<0>
TP_XDPPCH_OBSFN_B<1>
PCH_GPIO43
PCH_GPIO9
PCH_GPIO10
PM_LATRIGGER_L
ALL_SYS_PWRGD
PM_PWRBTN_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
SMBUS_PCH_DATA
SMBUS_PCH_CLK
JTAG_PCH_TCK

PCH OC0# PCH OC1# PCH OC2# PCH OC3# PCH OC4# PCH OC5# PCH OC6# PCH OC7#

OBSFN_A0 OBSFN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSFN_B0 OBSFN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSFN_C0 OBSFN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSFN_D0 OBSFN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

ISOLATE_CPU_MEM_L SMC_IG_THROTTLE_L FW_CLKREQ_L AP_CLKREQ_L SATARDRVR_A_EN SATARDRVR_B_EN TP_XDPPCH_OBSFN_D<0> TP_XDPPCH_OBSFN_D<1> SDCARD_RESET JTAG_GMUX_TCK AUD_IPHS_SWITCH_EN ME_TEMP_ALERT_L TP_XDPPCH_HOOK4 TP_XDPPCH_HOOK5 XDPPCH_PLTRST_L XDP_DBRESET_L JTAG_PCH_TDO TP_XDPPCH_TRST_L JTAG_PCH_TDI JTAG_PCH_TMS

PCH GPIO28 PCH GPIO0 PCH GPIO20 PCH GPIO18 PCH GPIO21 PCH GPIO19 PCH GPIO36 PCH GPIO37 PCH GPIO16 PCH GPIO49

1K series R on PCH Support Page

SYNC_MASTER=K18_MLB SYNC_DATE=06/22/2009

PAGE TITLE
eXtended Debug Port (XDP)

Apple Inc.

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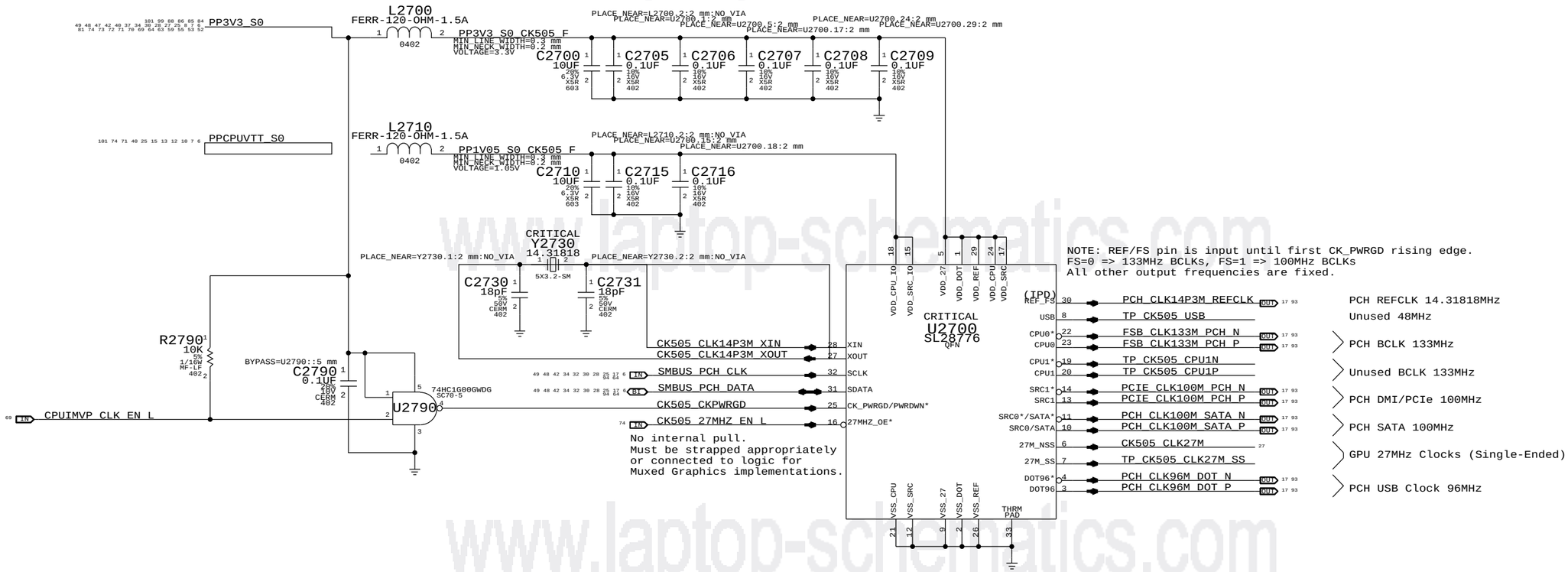

SYNC_MASTER=K17_REF SYNC_DATE=05/19/2009

PAGE TITLE: Clock (CK505)

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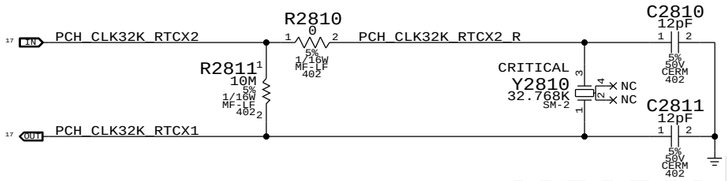
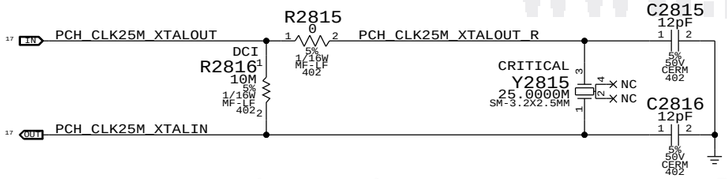
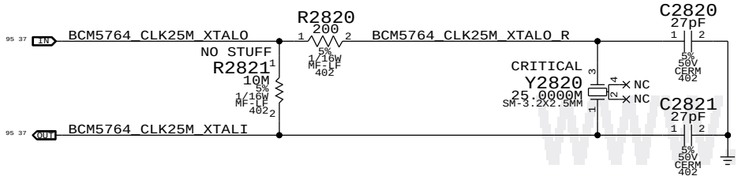
PCH RTC Crystal



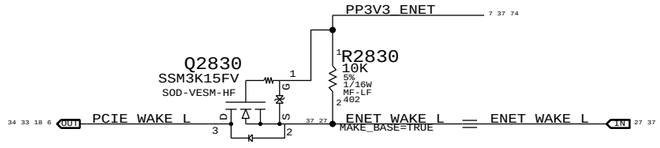
PCH 25MHz Crystal



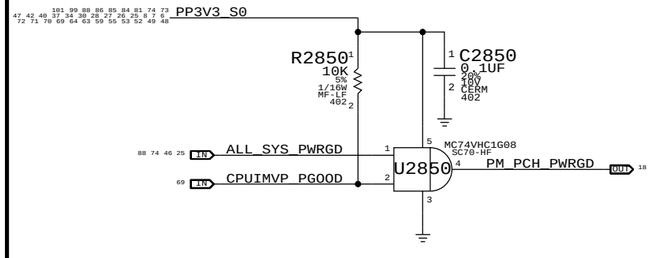
Caesar II (ENET) 25MHz Crystal



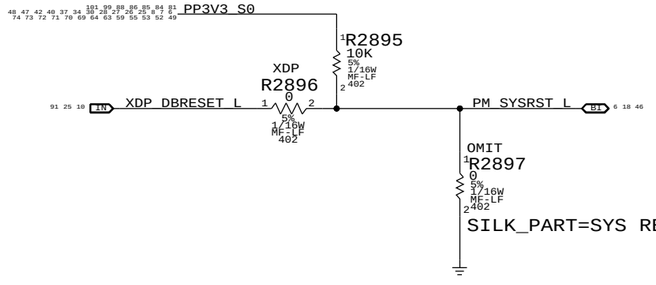
Ethernet WAKE# Isolation



PCH S0 PWRGD

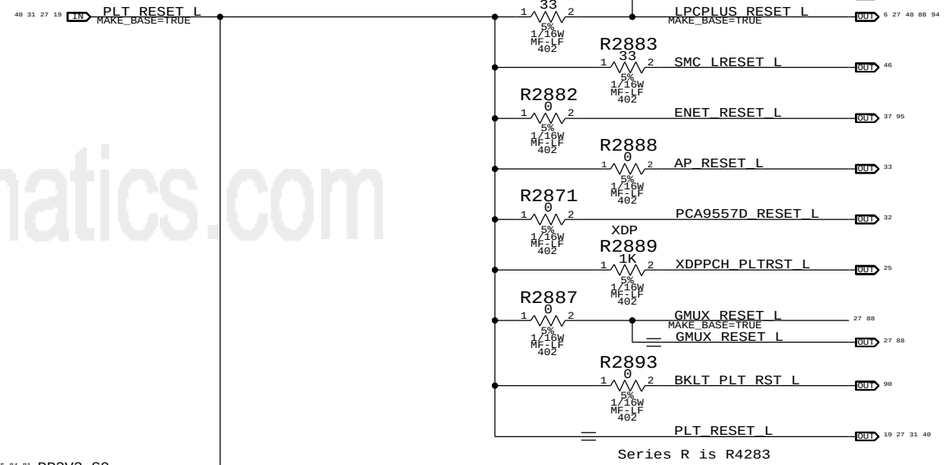


PCH Reset Button



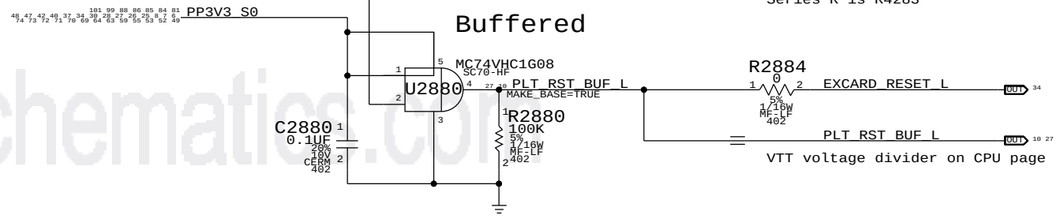
Platform Reset Connections

Unbuffered

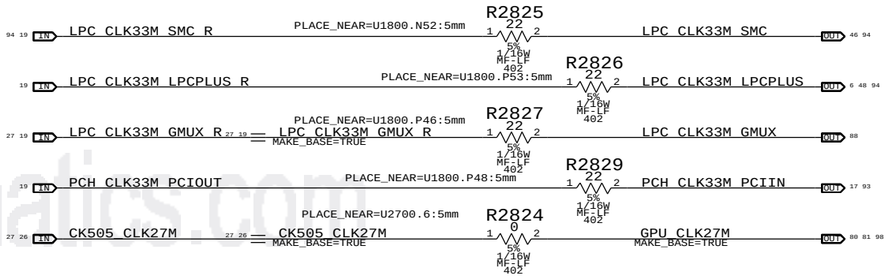


Series R is R4283

Buffered



VTT voltage divider on CPU page



SYNC_MASTER=K17_REF	SYNC_DATE=06/17/2009
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PP5PD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

73 68 31 30 7 PP1V5_S3

C2900 10UF 20% 6.3V X6S 603
C2901 10UF 20% 6.3V X6S 603
C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

32 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) F-RT-THB

73	CKE0		74	CKE1			
75	VDD		76	VDD			
77	NC	NC	78	A15	MEM_A_A<15>	IN	11 92
79	BA2	MEM_A_BA<2>	80	A14	MEM_A_A<14>	IN	11 92
81	VDD		82	VDD			
83	A12/BC*	MEM_A_A<12>	84	A11	MEM_A_A<11>	IN	11 92
85	A9	MEM_A_A<9>	86	A7	MEM_A_A<7>	IN	11 92
87	VDD		88	VDD			
89	A8	MEM_A_A<8>	90	A6	MEM_A_A<6>	IN	11 92
91	A5	MEM_A_A<5>	92	A4	MEM_A_A<4>	IN	11 92
93	VDD		94	VDD			
95	A3	MEM_A_A<3>	96	A2	MEM_A_A<2>	IN	11 92
97	A1	MEM_A_A<1>	98	A0	MEM_A_A<0>	IN	11 92
99	VDD		100	VDD			
101	CK0	MEM_A_CLK_P<0>	102	CK1	MEM_A_CLK_P<1>	IN	11 92
103	CK0*	MEM_A_CLK_N<0>	104	CK1*	MEM_A_CLK_N<1>	IN	11 92
105	VDD		106	VDD			
107	A10/AP	MEM_A_A<10>	108	BA1	MEM_A_BA<1>	IN	11 92
109	BA0	MEM_A_BA<0>	110	RAS*	MEM_A_RAS_L	IN	11 92
111	VDD		112	VDD			
113	WE*	MEM_A_WE_L	114	S0*	MEM_A_CS_L<0>	IN	11 92
115	CAS*	MEM_A_CAS_L	116	ODT0	MEM_A_ODT<0>	IN	11 92
117	VDD		118	VDD			
119	A13	MEM_A_A<13>	120	ODT1	MEM_A_ODT<1>	IN	11 92
121	S1*	MEM_A_CS_L<1>	122	NC			
123	VDD		124	VDD			
125	TEST		126	VREFCA			
127	VSS		128	VSS			
129	DQ32	=MEM_A_DQ<32>	130	DQ36	=MEM_A_DQ<36>	BI	29
131	DQ33	=MEM_A_DQ<33>	132	DQ37	MEM_A_DQ<37>	BI	11 29 92
133	VSS		134	VSS			
135	DQS4*	=MEM_A_DQS_N<4>	136	DM4	=MEM_A_DM<4>	IN	29
137	DQS4	=MEM_A_DQS_P<4>	138	VSS			
139	VSS		140	DQ38	=MEM_A_DQ<38>	BI	29
141	DQ34	=MEM_A_DQ<34>	142	DQ39	=MEM_A_DQ<39>	BI	29
143	DQ35	=MEM_A_DQ<35>	144	VSS			
145	VSS		146	DQ44	=MEM_A_DQ<44>	BI	29
147	DQ40	=MEM_A_DQ<40>	148	DQ45	=MEM_A_DQ<45>	BI	29
149	DQ41	=MEM_A_DQ<41>	150	VSS			
151	VSS		152	DQS5*	=MEM_A_DQS_N<5>	BI	29
153	DM5	=MEM_A_DM<5>	154	DQS5	=MEM_A_DQS_P<5>	BI	29
155	VSS		156	VSS			
157	DQ42	=MEM_A_DQ<42>	158	DQ46	=MEM_A_DQ<46>	BI	29
159	DQ43	=MEM_A_DQ<43>	160	DQ47	=MEM_A_DQ<47>	BI	29
161	VSS		162	VSS			
163	DQ48	=MEM_A_DQ<48>	164	DQ52	=MEM_A_DQ<52>	BI	29
165	DQ49	=MEM_A_DQ<49>	166	DQ53	=MEM_A_DQ<53>	BI	29
167	VSS		168	VSS			
169	DQS6*	=MEM_A_DQS_N<6>	170	DM6	=MEM_A_DM<6>	IN	29
171	DQS6	=MEM_A_DQS_P<6>	172	VSS			
173	VSS		174	DQ54	=MEM_A_DQ<54>	BI	29
175	DQ50	=MEM_A_DQ<50>	176	DQ55	=MEM_A_DQ<55>	BI	29
177	DQ51	=MEM_A_DQ<51>	178	VSS			
179	VSS		180	DQ60	=MEM_A_DQ<60>	BI	29
181	DQ56	=MEM_A_DQ<56>	182	DQ61	=MEM_A_DQ<61>	BI	29
183	DQ57	=MEM_A_DQ<57>	184	VSS			
185	VSS		186	DQS7*	=MEM_A_DQS_N<7>	BI	29
187	DM7	=MEM_A_DM<7>	188	DQS7	=MEM_A_DQS_P<7>	BI	29
189	VSS		190	VSS			
191	DQ58	=MEM_A_DQ<58>	192	DQ62	=MEM_A_DQ<62>	BI	29
193	DQ59	=MEM_A_DQ<59>	194	DQ63	=MEM_A_DQ<63>	BI	29
195	VSS		196	VSS			
197	SA0	MEM_A_SA<0>	198	EVENT*	MEM_EVENT_A_L	OUT	30 46 47
199	VDDSPD		200	SDA	SMBUS_PCH_DATA	BI	6 17 25 26 30 32 34 42 48 49 64 84
201	SA1	MEM_A_SA<1>	202	SCL	SMBUS_PCH_CLK	IN	6 17 25 26 30 32 34 42 48 49 64 84
203	VTT		204	VTT	PP0V75_S0_DDRVTT		7 30 31 68

KEY

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) CRITICAL F-RT-THB

1	VREFDQ		2	VSS			
3	VSS		4	DQ4	=MEM_A_DQ<4>	BI	29
5	DQ0	=MEM_A_DQ<0>	6	DQ5	=MEM_A_DQ<5>	BI	29
7	DQ1	=MEM_A_DQ<1>	8	VSS			
9	VSS		10	DQS0*	MEM_A_DQS_N<0>	BI	11 29 92
11	DM0	MEM_A_DM<0>	12	DQS0	MEM_A_DQS_P<0>	BI	11 29 92
13	VSS		14	VSS			
15	DQ2	=MEM_A_DQ<2>	16	DQ6	=MEM_A_DQ<6>	BI	29
17	DQ3	=MEM_A_DQ<3>	18	DQ7	=MEM_A_DQ<7>	BI	29
19	VSS		20	VSS			
21	DQ8	=MEM_A_DQ<8>	22	DQ12	=MEM_A_DQ<12>	BI	29
23	DQ9	=MEM_A_DQ<9>	24	DQ13	=MEM_A_DQ<13>	BI	29
25	VSS		26	VSS			
27	DQS1*	=MEM_A_DQS_N<1>	28	DM1	=MEM_A_DM<1>	IN	29
29	DQS1	=MEM_A_DQS_P<1>	30	RESET*	MEM_RESET_L	IN	30 31
31	VSS		32	VSS			
33	DQ10	=MEM_A_DQ<10>	34	DQ14	=MEM_A_DQ<14>	BI	29
35	DQ11	=MEM_A_DQ<11>	36	DQ15	=MEM_A_DQ<15>	BI	29
37	VSS		38	VSS			
39	DQ16	=MEM_A_DQ<16>	40	DQ20	=MEM_A_DQ<20>	BI	29
41	DQ17	=MEM_A_DQ<17>	42	DQ21	=MEM_A_DQ<21>	BI	29
43	VSS		44	VSS			
45	DQS2*	=MEM_A_DQS_N<2>	46	DM2	=MEM_A_DM<2>	IN	29
47	DQS2	=MEM_A_DQS_P<2>	48	VSS			
49	VSS		50	DQ22	=MEM_A_DQ<22>	BI	29
51	DQ18	=MEM_A_DQ<18>	52	DQ23	=MEM_A_DQ<23>	BI	29
53	DQ19	=MEM_A_DQ<19>	54	VSS			
55	VSS		56	DQ28	=MEM_A_DQ<28>	BI	29
57	DQ24	=MEM_A_DQ<24>	58	DQ29	=MEM_A_DQ<29>	BI	29
59	DQ25	=MEM_A_DQ<25>	60	VSS			
61	VSS		62	DQS3*	=MEM_A_DQS_N<3>	BI	29
63	DM3	=MEM_A_DM<3>	64	DQS3	=MEM_A_DQS_P<3>	BI	29
65	VSS		66	VSS			
67	DQ26	=MEM_A_DQ<26>	68	DQ30	=MEM_A_DQ<30>	BI	29
69	DQ27	=MEM_A_DQ<27>	70	DQ31	=MEM_A_DQ<31>	BI	29
71	VSS		72	VSS			

KEY

516-0229

PP0V75_S3_MEM_VREFCA_A 32

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

"Factory" (top) slot

SYNC_MASTER=K17_REF SYNC_DATE=05/13/2009

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

92 29 28 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_N<0>	11 28 29 92 92 30 29 11
92 29 28 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_P<0>	11 28 29 92 92 30 29 11
92 29 28 11	MEM_A_DM<0>	MAKE_BASE=TRUE	=	MEM_A_DM<0>	11 28 29 92 92 30 29 11
92 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>	28
92 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>	28
92 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>	28
92 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>	28
92 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>	28
92 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>	28
92 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>	28
92 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>	28

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

92 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>	28
92 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>	28
92 11	MEM_A_DM<1>	MAKE_BASE=TRUE	=	=MEM_A_DM<1>	28
92 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>	28
92 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>	28
92 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>	28
92 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>	28
92 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>	28
92 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>	28
92 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>	28
92 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=	=MEM_A_DQ<12>	28

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

92 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>	28
92 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>	28
92 11	MEM_A_DM<2>	MAKE_BASE=TRUE	=	=MEM_A_DM<2>	28
92 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>	28
92 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>	28
92 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>	28
92 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>	28
92 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>	28
92 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>	28
92 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<17>	28
92 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>	28

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

92 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>	28
92 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>	28
92 11	MEM_A_DM<3>	MAKE_BASE=TRUE	=	=MEM_A_DM<3>	28
92 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>	28
92 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>	28
92 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>	28
92 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<24>	28
92 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>	28
92 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>	28
92 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>	28
92 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>	28

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

92 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>	28
92 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>	28
92 11	MEM_A_DM<4>	MAKE_BASE=TRUE	=	=MEM_A_DM<4>	28
92 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<33>	28
92 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>	28
92 29 28 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	=	MEM_A_DQ<37>	11 28 29 92 92 30 29 11
92 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>	28
92 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>	28
92 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>	28
92 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>	28
92 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>	28

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

92 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>	28
92 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>	28
92 11	MEM_A_DM<5>	MAKE_BASE=TRUE	=	=MEM_A_DM<5>	28
92 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>	28
92 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>	28
92 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<45>	28
92 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>	28
92 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>	28
92 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>	28
92 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>	28
92 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>	28

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

92 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>	28
92 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>	28
92 11	MEM_A_DM<6>	MAKE_BASE=TRUE	=	=MEM_A_DM<6>	28
92 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>	28
92 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>	28
92 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>	28
92 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>	28
92 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>	28
92 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>	28
92 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>	28
92 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>	28

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

92 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>	28
92 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>	28
92 11	MEM_A_DM<7>	MAKE_BASE=TRUE	=	=MEM_A_DM<7>	28
92 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>	28
92 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>	28
92 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>	28
92 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<61>	28
92 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>	28
92 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>	28
92 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>	28
92 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>	28

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

92 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_N<0>	11 29 30 92
92 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_P<0>	11 29 30 92
92 11	MEM_B_DM<0>	MAKE_BASE=TRUE	=	MEM_B_DM<0>	11 29 30 92
92 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>	30
92 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>	30
92 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>	30
92 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>	30
92 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>	30
92 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>	30
92 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>	30
92 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=	=MEM_B_DQ<0>	30

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

92 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>	30
92 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>	30
92 11	MEM_B_DM<1>	MAKE_BASE=TRUE	=	=MEM_B_DM<1>	30
92 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>	30
92 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>	30
92 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>	30
92 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>	30
92 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>	30
92 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>	30
92 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>	30
92 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=	=MEM_B_DQ<9>	30

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

92 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>	30
92 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>	30
92 11	MEM_B_DM<2>	MAKE_BASE=TRUE	=	=MEM_B_DM<2>	30
92 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>	30
92 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>	30
92 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>	30
92 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>	30
92 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>	30
92 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>	30
92 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>	30
92 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>	30

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

92 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>	30
92 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>	30
92 11	MEM_B_DM<3>	MAKE_BASE=TRUE	=	=MEM_B_DM<3>	30
92 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>	30
92 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>	30
92 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>	30
92 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>	30
92 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>	30
92 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>	30
92 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>	30
92 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>	30

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

92 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>	30
92 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>	30
92 11	MEM_B_DM<4>	MAKE_BASE=TRUE	=	=MEM_B_DM<4>	30
92 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>	30
92 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>	30
92 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	=	MEM_B_DQ<37>	11 29 30 92
92 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>	30
92 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>	30
92 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>	30
92 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>	30
92 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>	30

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

92 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>	30
92 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>	30
92 11	MEM_B_DM<5>	MAKE_BASE=TRUE	=	=MEM_B_DM<5>	30
92 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>	30
92 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>	30
92 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>	30
92 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>	30
92 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>	30
92 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>	30
92 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>	30
92 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>	30

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

92 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>	30
92 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>	30
92 11	MEM_B_DM<6>	MAKE_BASE=TRUE	=	=MEM_B_DM<6>	30
92 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>	30
92 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>	30
92 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>	30
92 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>	30
92 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>	30
92 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>	30
92 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>	30
92 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>	30

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

92 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>	30
92 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>	30
92 11	MEM_B_DM<7>	MAKE_BASE=TRUE	=	=MEM_B_DM<7>	30
92 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>	30
92 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>	30
92 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>	30
92 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>	30
92 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>	30
92 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>	30
92 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>	30
92 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>	30

SYNC_MASTER=K18_MLB SYNC_DATE=06/19/2009

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

73 68 31 28 7 PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X6S 603
C3101 10UF 20% 6.3V X6S 603

32 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

DDR3-SODIMM (2 OF 2)
OMIT J3100 F-RT-BGA6
KEY

92 11 IN MEM_B_CKE<0>	73 CKE0	CKE1 74	MEM_B_CKE<1> IN 11 92
	75 VDD	VDD 76	
92 11 IN MEM_B_BA<2>	77 NC	A15 78	MEM_B_A<15> IN 11 92
	79 BA2	A14 80	MEM_B_A<14> IN 11 92
	81 VDD	VDD 82	
92 11 IN MEM_B_A<12>	83 A12/BC*	A11 84	MEM_B_A<11> IN 11 92
92 11 IN MEM_B_A<9>	85 A9	A7 86	MEM_B_A<7> IN 11 92
	87 VDD	VDD 88	
92 11 IN MEM_B_A<8>	89 A8	A6 90	MEM_B_A<6> IN 11 92
92 11 IN MEM_B_A<5>	91 A5	A4 92	MEM_B_A<4> IN 11 92
	93 VDD	VDD 94	
92 11 IN MEM_B_A<3>	95 A3	A2 96	MEM_B_A<2> IN 11 92
92 11 IN MEM_B_A<1>	97 A1	A0 98	MEM_B_A<0> IN 11 92
	99 VDD	VDD 100	
92 11 IN MEM_B_CLK_P<0>	101 CK0	CK1 102	MEM_B_CLK_P<1> IN 11 92
92 11 IN MEM_B_CLK_N<0>	103 CK0*	CK1* 104	MEM_B_CLK_N<1> IN 11 92
	105 VDD	VDD 106	
92 11 IN MEM_B_A<10>	107 A10/AP	BA1 108	MEM_B_BA<1> IN 11 92
92 11 IN MEM_B_BA<0>	109 BA0	RAS* 110	MEM_B_RAS_L IN 11 92
	111 VDD	VDD 112	
92 11 IN MEM_B_WE_L	113 WE*	S0* 114	MEM_B_CS_L<0> IN 11 92
92 11 IN MEM_B_CAS_L	115 CAS*	ODT0 116	MEM_B_ODT<0> IN 11 92
	117 VDD	VDD 118	
92 11 IN MEM_B_A<13>	119 A13	ODT1 120	MEM_B_ODT<1> IN 11 92
92 11 IN MEM_B_CS_L<1>	121 S1*	NC 122	*NC
	123 VDD	VDD 124	
	125 TEST	VREFCA 126	
	127 VSS	VSS 128	
29 BI =MEM_B_DQ<32>	129 DQ32	DQ36 130	=MEM_B_DQ<36> BI 29
29 BI =MEM_B_DQ<33>	131 DQ33	DQ37 132	=MEM_B_DQ<37> BI 29
	133 VSS	VSS 134	
29 BI =MEM_B_DQS_N<4>	135 DQS4*	DM4 136	=MEM_B_DM<4> IN 29
29 BI =MEM_B_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	=MEM_B_DQ<38> BI 29
92 29 11 BI MEM_B_DQ<37>	141 DQ34	DQ39 142	=MEM_B_DQ<39> BI 29
29 BI =MEM_B_DQ<35>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	=MEM_B_DQ<44> BI 29
29 BI =MEM_B_DQ<40>	147 DQ40	DQ45 148	=MEM_B_DQ<45> BI 29
29 BI =MEM_B_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	=MEM_B_DQS_N<5> BI 29
29 IN =MEM_B_DM<5>	153 DM5	DQS5 154	=MEM_B_DQS_P<5> BI 29
	155 VSS	VSS 156	
29 BI =MEM_B_DQ<42>	157 DQ42	DQ46 158	=MEM_B_DQ<46> BI 29
29 BI =MEM_B_DQ<43>	159 DQ43	DQ47 160	=MEM_B_DQ<47> BI 29
	161 VSS	VSS 162	
29 BI =MEM_B_DQ<48>	163 DQ48	DQ52 164	=MEM_B_DQ<52> BI 29
29 BI =MEM_B_DQ<49>	165 DQ49	DQ53 166	=MEM_B_DQ<53> BI 29
	167 VSS	VSS 168	
29 BI =MEM_B_DQS_N<6>	169 DQS6*	DM6 170	=MEM_B_DM<6> IN 29
29 BI =MEM_B_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	=MEM_B_DQ<54> BI 29
29 BI =MEM_B_DQ<50>	175 DQ50	DQ55 176	=MEM_B_DQ<55> BI 29
29 BI =MEM_B_DQ<51>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	=MEM_B_DQ<60> BI 29
29 BI =MEM_B_DQ<56>	181 DQ56	DQ61 182	=MEM_B_DQ<61> BI 29
29 BI =MEM_B_DQ<57>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	=MEM_B_DQS_N<7> BI 29
29 IN =MEM_B_DM<7>	187 DM7	DQS7 188	=MEM_B_DQS_P<7> BI 29
	189 VSS	VSS 190	
29 BI =MEM_B_DQ<58>	191 DQ58	DQ62 192	=MEM_B_DQ<62> BI 29
29 BI =MEM_B_DQ<59>	193 DQ59	DQ63 194	=MEM_B_DQ<63> BI 29
	195 VSS	VSS 196	
MEM_B_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_A_L OUT 28 46 47
	199 VDDSPD	SDA 200	SMBUS_PCH_DATA BI 8,17 25 26 28 32 34 42 48 49 64 94
MEM_B_SA<1>	201 SA1	SCL 202	SMBUS_PCH_CLK IN 8,17 25 26 28 32 34 42 48 49 64 94
	203 VTT	VTT 204	PP0V75_S0_DDRVTT 7 28 31 68
	MTG PINS		
	205 MTG PIN	MTG PIN 206	
	207 MTG PIN	MTG PIN 208	
	209 MTG PIN	MTG PIN 210	
	211 MTG PIN	MTG PIN 212	

516s0806
SPD ADDR=0xA4(WR)/0xA5(RD)

R3140 10K 5% 1/16W MF-LF 402
R3141 10k 5% 1/16W MF-LF 402
C3140 2.2UF 20% 6.3V CERM 402-LF

70 69 64 63 31 29 PP3V3_S0

DDR3-SODIMM (1 OF 2)
OMIT CRITICAL J3100 F-RT-BGA6
KEY

	1 VREFDQ	VSS 2	
	3 VSS	DQ4 4	=MEM_B_DQ<4> BI 29
29 BI =MEM_B_DQ<0>	5 DQ0	DQ5 6	=MEM_B_DQ<5> BI 29
29 BI =MEM_B_DQ<1>	7 DQ1	VSS 8	
	9 VSS	DQS0* 10	MEM_B_DQS_N<0> BI 11 29 92
92 29 11 IN MEM_B_DM<0>	11 DM0	DQS0 12	MEM_B_DQS_P<0> BI 11 29 92
	13 VSS	VSS 14	
29 BI =MEM_B_DQ<2>	15 DQ2	DQ6 16	=MEM_B_DQ<6> BI 29
29 BI =MEM_B_DQ<3>	17 DQ3	DQ7 18	=MEM_B_DQ<7> BI 29
	19 VSS	VSS 20	
29 BI =MEM_B_DQ<8>	21 DQ8	DQ12 22	=MEM_B_DQ<12> BI 29
29 BI =MEM_B_DQ<9>	23 DQ9	DQ13 24	=MEM_B_DQ<13> BI 29
	25 VSS	VSS 26	
29 BI =MEM_B_DQS_N<1>	27 DQS1*	DM1 28	=MEM_B_DM<1> IN 29
29 BI =MEM_B_DQS_P<1>	29 DQS1	RESET* 30	MEM_RESET_L IN 28 31
	31 VSS	VSS 32	
29 BI =MEM_B_DQ<10>	33 DQ10	DQ14 34	=MEM_B_DQ<14> BI 29
29 BI =MEM_B_DQ<11>	35 DQ11	DQ15 36	=MEM_B_DQ<15> BI 29
	37 VSS	VSS 38	
29 BI =MEM_B_DQ<16>	39 DQ16	DQ20 40	=MEM_B_DQ<20> BI 29
29 BI =MEM_B_DQ<17>	41 DQ17	DQ21 42	=MEM_B_DQ<21> BI 29
	43 VSS	VSS 44	
29 BI =MEM_B_DQS_N<2>	45 DQS2*	DM2 46	=MEM_B_DM<2> IN 29
29 BI =MEM_B_DQS_P<2>	47 DQS2	VSS 48	
	49 VSS	DQ22 50	=MEM_B_DQ<22> BI 29
29 BI =MEM_B_DQ<18>	51 DQ18	DQ23 52	=MEM_B_DQ<23> BI 29
29 BI =MEM_B_DQ<19>	53 DQ19	VSS 54	
	55 VSS	DQ28 56	=MEM_B_DQ<28> BI 29
29 BI =MEM_B_DQ<24>	57 DQ24	DQ29 58	=MEM_B_DQ<29> BI 29
29 BI =MEM_B_DQ<25>	59 DQ25	VSS 60	
	61 VSS	DQS3* 62	=MEM_B_DQS_N<3> BI 29
29 IN =MEM_B_DM<3>	63 DM3	DQS3 64	=MEM_B_DQS_P<3> BI 29
	65 VSS	VSS 66	
29 BI =MEM_B_DQ<26>	67 DQ26	DQ30 68	=MEM_B_DQ<30> BI 29
29 BI =MEM_B_DQ<27>	69 DQ27	DQ31 70	=MEM_B_DQ<31> BI 29
	71 VSS	VSS 72	

516s0806

PP0V75_S3_MEM_VREFCA_B 32

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009
PAGE TITLE: DDR3 SO-DIMM Connector B
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH
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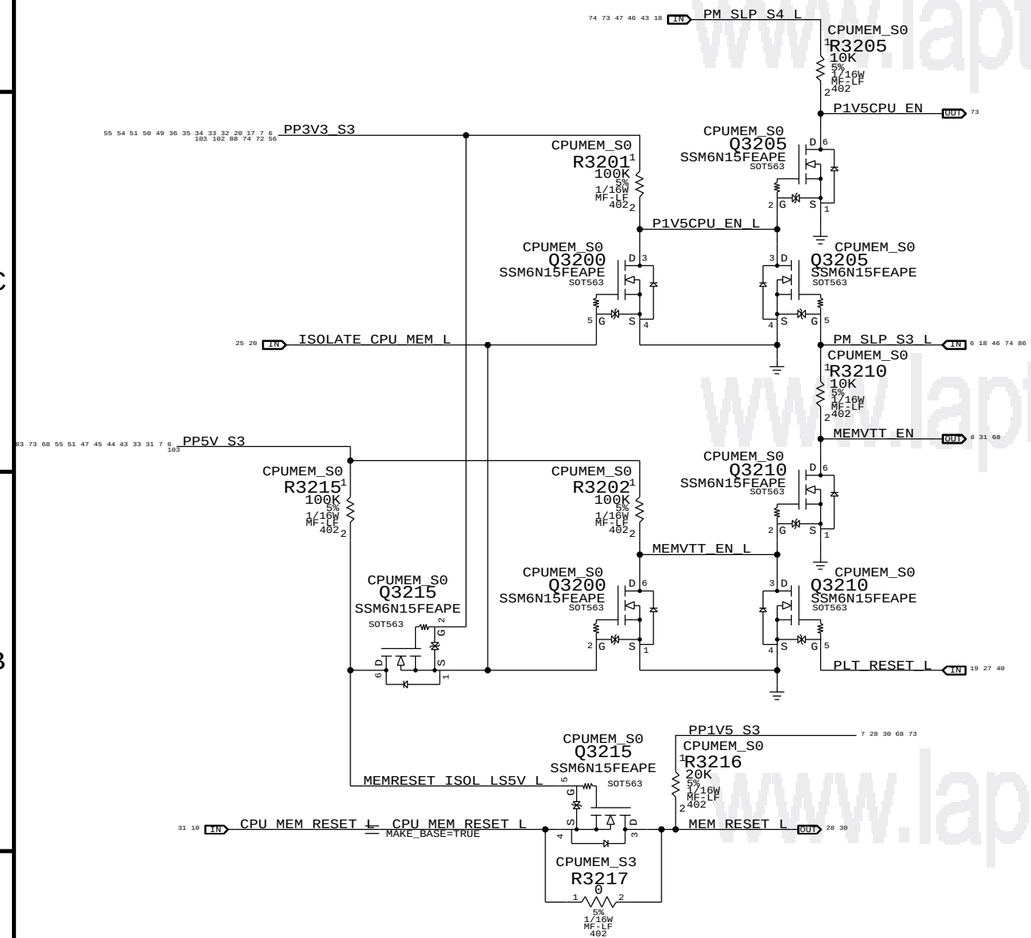
SHEET 30 OF 103

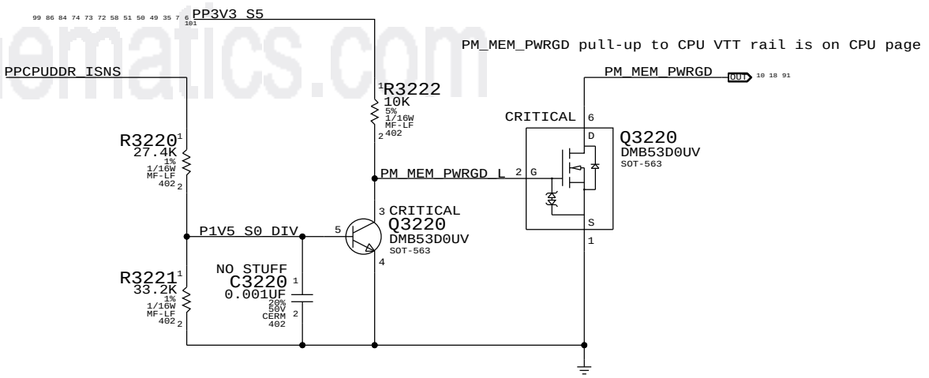
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

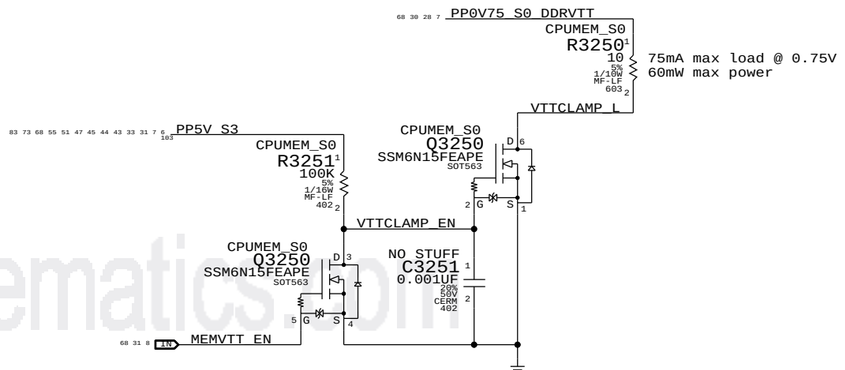


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K18_MLB SYNC_DATE=10/14/2009

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

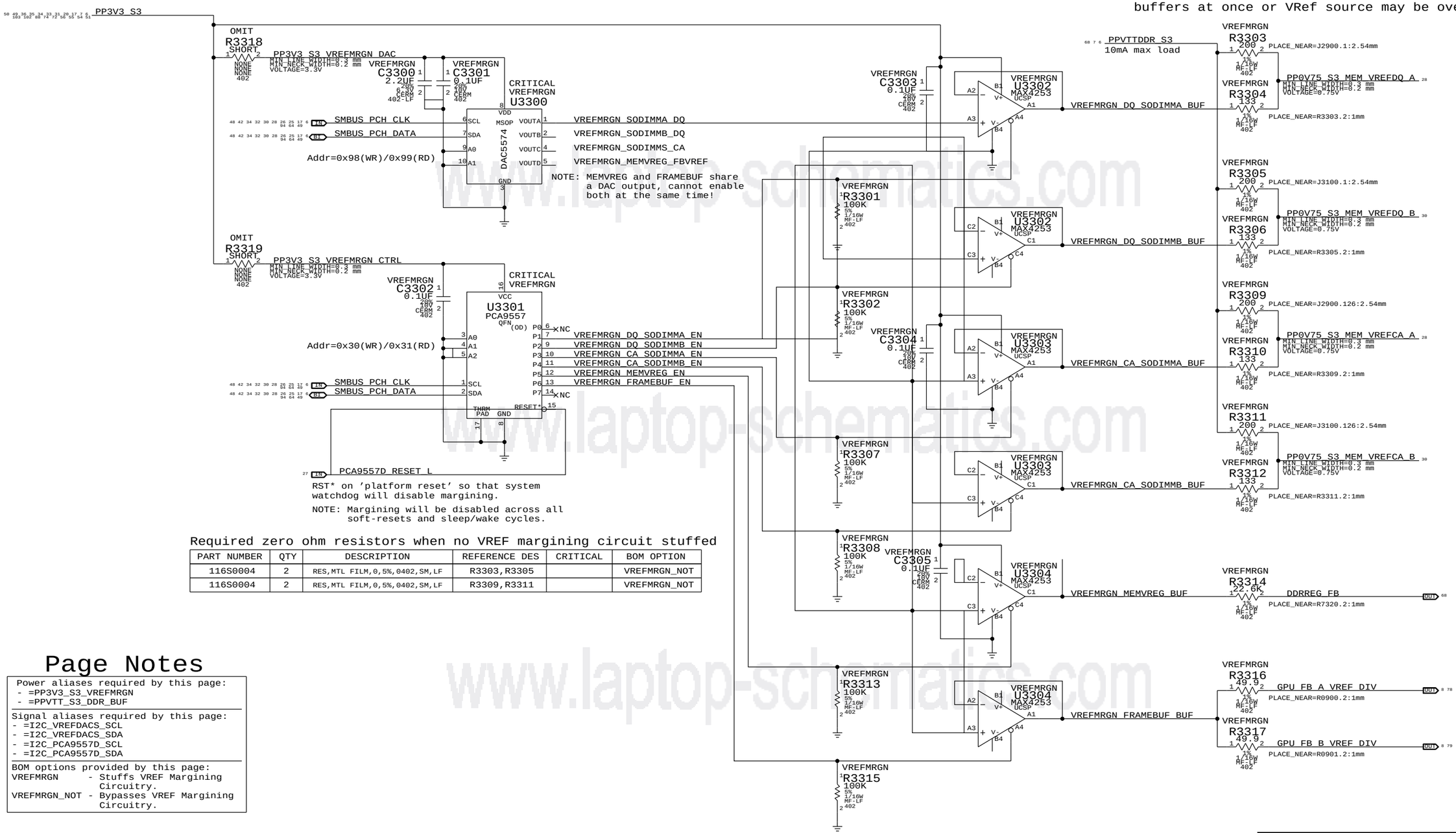
DRAWING NUMBER: | SIZE: D

REVISION:

BRANCH:

PAGE: 32 OF 132

SHEET: 31 OF 103



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

PAGE: 33 OF 132

SHEET: 32 OF 103

AP_PWR_EN

AP_CLKREQ_L

Q3401
SSM6N15FEAPE
SOT563

AP_CLKREQ_Q_L

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

727 MA PEAK
606 MA NOMINAL MAX

155S0367
L3404
FERR-120-OHM-3A
0603

CRITICAL
R3452
0.002
1%
1/2W
1206

CRITICAL
Q3450
TPCP8102
23V1K-SM

PP3V3_WLAN
PP3V3_WLAN_F
PP3V3_WLAN_R
PP3V3_S3

C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 10% 10V CERM 402
C3420 10UF 20% 10V X5R 805
C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 33K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.

ISNS_AIRPORT_P
ISNS_AIRPORT_N

PM_WLAN_EN_L

516S0582
CRITICAL
J3401
500913-0302
F-ST-SM

PCIE_AP_R2D_P
PCIE_AP_R2D_N
C3431 0.1uF 10% 16V X5R 402
C3430 0.1uF 10% 16V X5R 402
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N

PCIE_AP_D2R_P
PCIE_AP_D2R_N

AIRPORT

CRITICAL
L3401
90-OHM-100MA
DLP11S

PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N

BLUETOOTH

L3403
90-OHM CRITICAL
DLP0NS
PLACE_NEAR=J3401.21:2.54MM

CONN_USB2_BT_P
CONN_USB2_BT_N
USB_BT_P
USB_BT_N

PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3432 0.01UF 10% 10V CERM 402

L3406
FERR-120-OHM-1.5A
0402-LF
PLACE L3406 NEAR J3401.

PCIE_WAKE_L

RC (R3453 AND C3453)VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN
3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET

PP3V3_WLAN_F
PP3V3_S3
R3453 110K 5% 1/16W MF-LF 402
U3402
74LVC1G17
SOT353-1
TC7SZ08AFEAPE
SOT665
U3401
WLAN_SMIT_BUF
AP_RESET_CONN_L
AP_RESET_L
R3455 1 5% 1/16W MF-LF 402
WLAN_SMIT_RC
WLAN_SMIT_DISCHRG
C3453 1UF 10% 6.3V CERM 402
R3454 62K 5% 1/16W MF-LF 402 NOSTUFF
Q3401
SSM6N15FEAPE
SOT563

CRITICAL
J3402 518S0767
819Q-3506-K281
F-RT-SM

PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

ALS
CAMERA

CRITICAL
L3407
90-OHM
DLP0NS
PLACE_NEAR=J3402.6:2.54MM
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3402

275 mA peak
206 mA nominal max

L3408
FERR-120-OHM-1.5A
0402-LF
PLACEMENT_NOTE=Place close to J3402
PP5V_S3
C3452 0.1uF 20% 10V CERM 402

SYNC_MASTER=K18_MLB
SYNC_DATE=06/19/2009
PAGE TITLE
X16/ALS/CAMERA CONNECTOR
Apple Inc.
DRAWING NUMBER
SIZE D
REVISION
BRANCH
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EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

PP3V3_S3
- C3530 0.1uF 20% 10V CERM 402
- C3531 10uF 20% 6.3V X5R 603

PP1V5_S0
- C3534 0.1uF 20% 10V CERM 402
- C3535 10uF 20% 6.3V X5R 603

L3502
90-OHM DLP0NS

USB_EXCARD_N — MAKE_BASE=TRUE — USB2_EXCARD_CONN_N
USB_EXCARD_P — MAKE_BASE=TRUE — USB2_EXCARD_CONN_P
PLACE_NEAR=J3500.3:4mm

L3503
90-OHM-100MA DLP11S

PCIE_CLK100M_EXCARD_N — PCIE_CLK100M_EXCARD_CONN_N
PCIE_CLK100M_EXCARD_P — PCIE_CLK100M_EXCARD_CONN_P
PLACE_NEAR=J3500.19:4mm

PLACE_NEAR=J3500.24:4mm

PCIE_EXCARD_R2D_C_N — C3571 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_N
PCIE_EXCARD_R2D_C_P — C3570 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_P
PLACE_NEAR=J3500.25:4mm

CRITICAL
J3500
502250-8627
518S0647

PCIE_EXCARD_R2D_N	24	25	PCIE_EXCARD_R2D_P
PCIE_EXCARD_D2R_P	22	23	
	20	21	PCIE_EXCARD_D2R_N
PCIE_CLK100M_EXCARD_CONN_N	18	19	PCIE_CLK100M_EXCARD_CONN_P
EXCARD_CLKREQ_CONN_L	16	17	EXCARD_CPPE_L
PP3V3_S0_EXCARD_SWITCH	14	15	PP3V3_S0_EXCARD_SWITCH
PP3V3_S3_EXCARD_SWITCH	12	13	PLT_RESET_SWITCH_L
PP1V5_S0_EXCARD_SWITCH	10	11	PCIE_WAKE_L
SMBUS_PCH_DATA	8	9	PP1V5_S0_EXCARD_SWITCH
	6	7	SMBUS_PCH_CLK
EXCARD_CPUSB_L	4	5	NC
USB2_EXCARD_CONN_N	2	3	USB2_EXCARD_CONN_P
	1		

NC × 2

PP3V3_S3 — OMIT R3504 SHORT — PP3V3_S3_EXCARD_R
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=3.3V

PP3V3_S0 — OMIT R3503 SHORT — PP3V3_S0_EXCARD_R
MIN_LINE_WIDTH=0.3mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

PP1V5_S0 — OMIT R3502 SHORT — PP1V5_S0_EXCARD_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V

CRITICAL
U3500
TPS2231
QFN

	17 AUXIN	AUXOUT 15	PP3V3_S3_EXCARD_SWITCH
PP3V3_S3	2 VIN3P3	VOUT3P3 3	
PP1V5_S0	12 VIN1P5	VOUT1P5 11	
SMC_EXCARD_PWR_EN	20 SHDN*	PERST* 8	PLT_RESET_SWITCH_L
TP_EXCARD_STBY_L	1 STBY*	CPPE* 10	EXCARD_CPPE_L
EXCARD_RESET_L	6 SYSRST*	CPUSB* 9	EXCARD_CPUSB_L
EXCARD_OC_L	19 OC*	(IPU)	
NC	4 NC0	RCLKEN (IPU) 18	EXCARD_RCLKEN
NC	5 NC1		
NC	13 NC2		
NC	14 NC3		
NC	16 NC4	THRML_PAD 21	
		GND 7	

VOLTAGE=3.3V, MIN_LINE_WIDTH=.3mm, MIN_NECK_WIDTH=0.2mm — PP3V3_S3_EXCARD_SWITCH — C3500 0.1uF 20% 10V CERM 402 — C3503 10uF 20% 6.3V X5R 603

VOLTAGE=3.3V, MIN_LINE_WIDTH=.6mm, MIN_NECK_WIDTH=0.2mm — PP3V3_S0_EXCARD_SWITCH — C3501 0.1uF 20% 10V CERM 402 — C3504 10uF 20% 6.3V X5R 603

VOLTAGE=1.5V, MIN_LINE_WIDTH=.6mm, MIN_NECK_WIDTH=0.11mm — PP1V5_S0_EXCARD_SWITCH — C3502 0.1uF 20% 10V CERM 402 — C3505 10uF 20% 6.3V X5R 603

SMC_EXCARD R3500 0 5% 1/16W MF-LF 402 — EXCARD_SHDN_L_R

All pull-ups to AUXIN rail

PP3V3_S3 — C3550 0.1uF 20% 10V CERM 402

SMC_EXCARD_NOT R3550 0 5% 1/16W MF-LF 402

SMC_EXCARD R3551 0 5% 1/16W MF-LF 402 — SMC_EXCARD_CP

EXCARD_CPUSB_L, EXCARD_CPPE_L — U3551 74HC1G00GWDG SC70-5 — EXCARD_CP

OUTPUT DECOUPLING

PP3V3_S0 — EXCARD_RCLKEN — U3560 74HC1G00GWDG SC70-5 — EXCARD_CLKREQ_L

R3561 100K 1% 1/16W MF-LF 402 — EXCARD_CLKREQ_CONN — U3561 SN74LVC1G04YZPR BGA — C3560 0.1uF 20% 10V CERM 402 — EXCARD_CLKREQ_CONN_L

SYNC_MASTER=K17_WFERRY	SYNC_DATE=06/09/2009	
PAGE TITLE: ExpressCard Connector		
Apple Inc.	DRAWING NUMBER	SIZE D
	REVISION	
	BRANCH	
	PAGE	35 OF 132
	SHEET	34 OF 103

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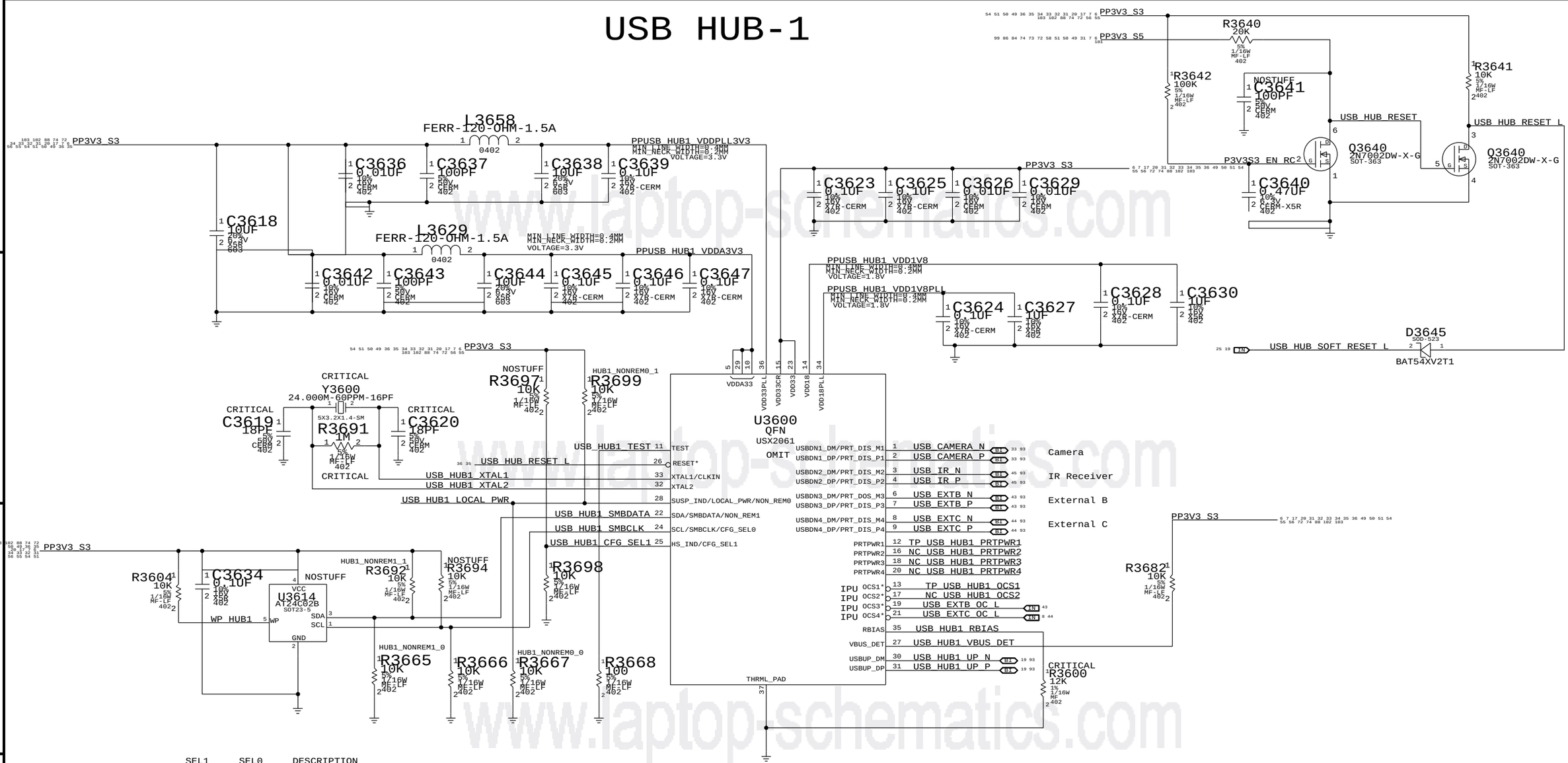
USB HUB-1



SEL1	SEL0	DESCRIPTION
0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	IC,ASSP,USB2.0,HUB CNTROL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	IC,USB2514B,USB 2.0,HUB CNTRL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	IC,USX2061,USB 2.0,HUB CNTRL,4 PRT,36QFN	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC_MASTER=K18_MLB SYNC_DATE=10/07/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER | SIZE: D

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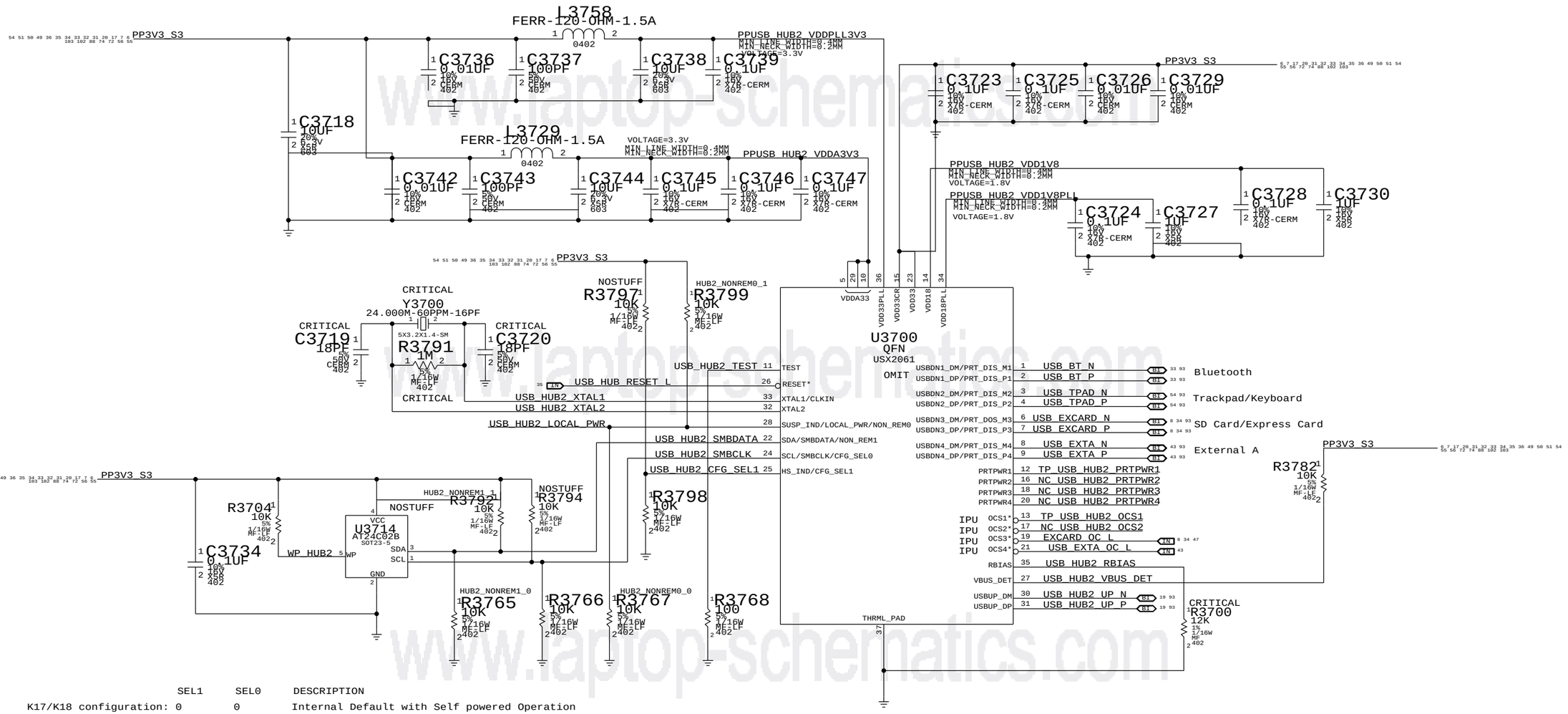
USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/09/2009

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: D

SIZE

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BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

PP3V3_ENET
86mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-0.5A
CRITICAL L3905 FERR-600-OHM-0.5A
CRITICAL L3910 FERR-600-OHM-0.5A

PP3V3_ENET_PHY_XTALVDDH
PP3V3_ENET_PHY_BIASVDDH
PP3V3_ENET_PHY_AVDDH

BCM57765 R3915 0 5% 1/16W MF-LF 402
BCM57765 R3900 0 5% 1/16W MF-LF 402
C3900 0.1UF 10% 16V X7R-CERM 402
C3905 0.1UF 10% 16V X7R-CERM 402
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDO_PIN20
BCM57765_XTALVDDH
BCM57765_SR_LX
BCM57765_SR_VFB

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603
PP1V2_ENET
396mA (1000base-T, Caesar II)

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

BCM57765 R3940 4.7K 5% 1/16W MF-LF 402
BCM57765 R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402
C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

AVDDH BIASVDDH VDDC VDDIO XTALVDDH VDDIO VDDC REGCTL12 VDDIO WAKE* AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC VDDC

PP3V3_S0
BCM57765 R3942 1K 5% 1/16W MF-LF 402

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402
BCM57765 R3943 0 5% 1/16W MF-LF 402

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
(IPU)
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

BCM57765 R3965 1.24K 1% 1/16W MF-LF 402

THRM_PAD 69

CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2

TRD0_P ENET_MDI_P<0>
TRD0_N ENET_MDI_N<0>
TRD1_P ENET_MDI_P<1>
TRD1_N ENET_MDI_N<1>
TRD2_P ENET_MDI_P<2>
TRD2_N ENET_MDI_N<2>
TRD3_P ENET_MDI_P<3>
TRD3_N ENET_MDI_N<3>

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

(IPD) GPIO_0/SERIAL_DO NC
GPIO_1/SERIAL_DI NC
PP3V3R1V8_SW_SD_VIO
GPIO_2 BCM57765_MEDIA_SENSE R3972 0 5% 1/16W MF-LF 402 BCM57765 ENET_ENERGY_DET
NC NC
PCIE_VDDL BCM57765_CR_CMD
DC0 NC
DC4 NC
DC3 NC
DC2 NC
DC1 NC
NC NC
VMAIN_PRSNT BCM57765_CR_DATA<5>
VAUX_PRSNT BCM57765_CR_DATA<6>
VDDC BCM57765_CR_DATA<7>
SMB_CLK BCM57765_CE_L_MS_INS_L
ENERGY_DET BCM57765_CR_LED
DC5 NC
SPD1000LED* TP_BCM57765_XD_DET

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF 10% 16V X7R-CERM 402
U3990 AT45DB011D SOIC-8S1 OMIT
VCC SCK CS* WP* RESET* GND SI SO
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
BCM57765 R3990 4.7K 5% 1/16W MF-LF 402
BCM5764M R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_LED	R3980	0	ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0	ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K	PP3V3_S0
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K	PP3V3_ENET
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K	
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K	
16-VDDIO	BCM57765_SR_LX	R3986	0	
20-XTALVDDH	BCM57765_VDDO_PIN20	R3987	0	PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0	PP1V2_ENET
17-VDDC	BCM57765_XTALVDDH	R3989	0	
14-VDDC	BCM57765_SR_VDD	R3998	0	
06-VDDC	BCM57765_SMB_CLK	R3999	0	

All: 5% 1/16W MF-LF 402

26-PCIE_VDDL BCM57765_CR_CMD PLACE_NEAR=U3900.26:4 mm
L3999 FERR-600-OHM-0.5A SM CRITICAL
Keep net short, with no stubs.
BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 PLACE_NEAR=U3900.26:4 mm
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 PLACE_NEAR=L3999.1:4 mm

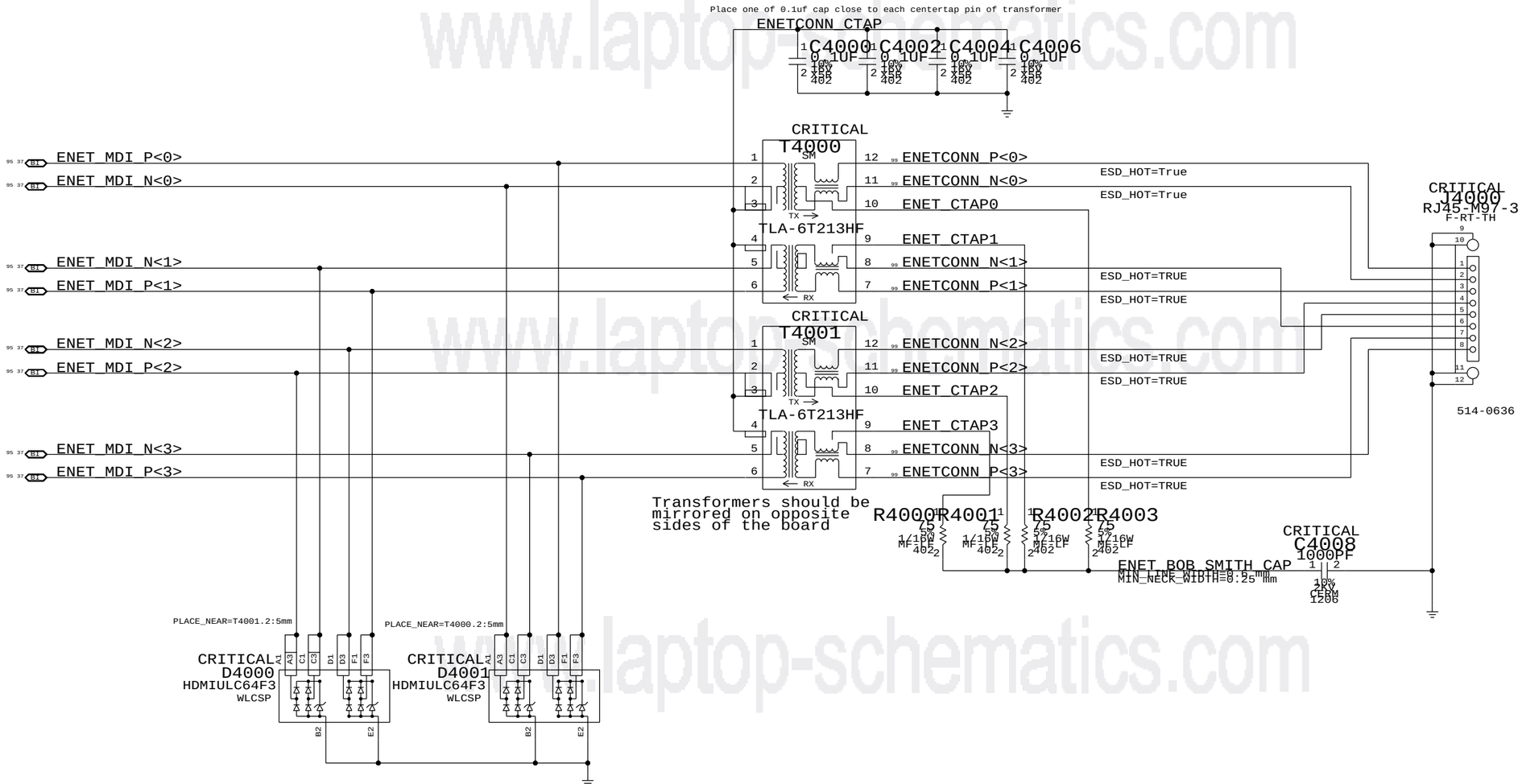
SYNC_MASTER=K18_MLB SYNC_DATE=10/28/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER: SIZE D
REVISION:
BRANCH:
PAGE: 39 OF 132
SHEET: 37 OF 103

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

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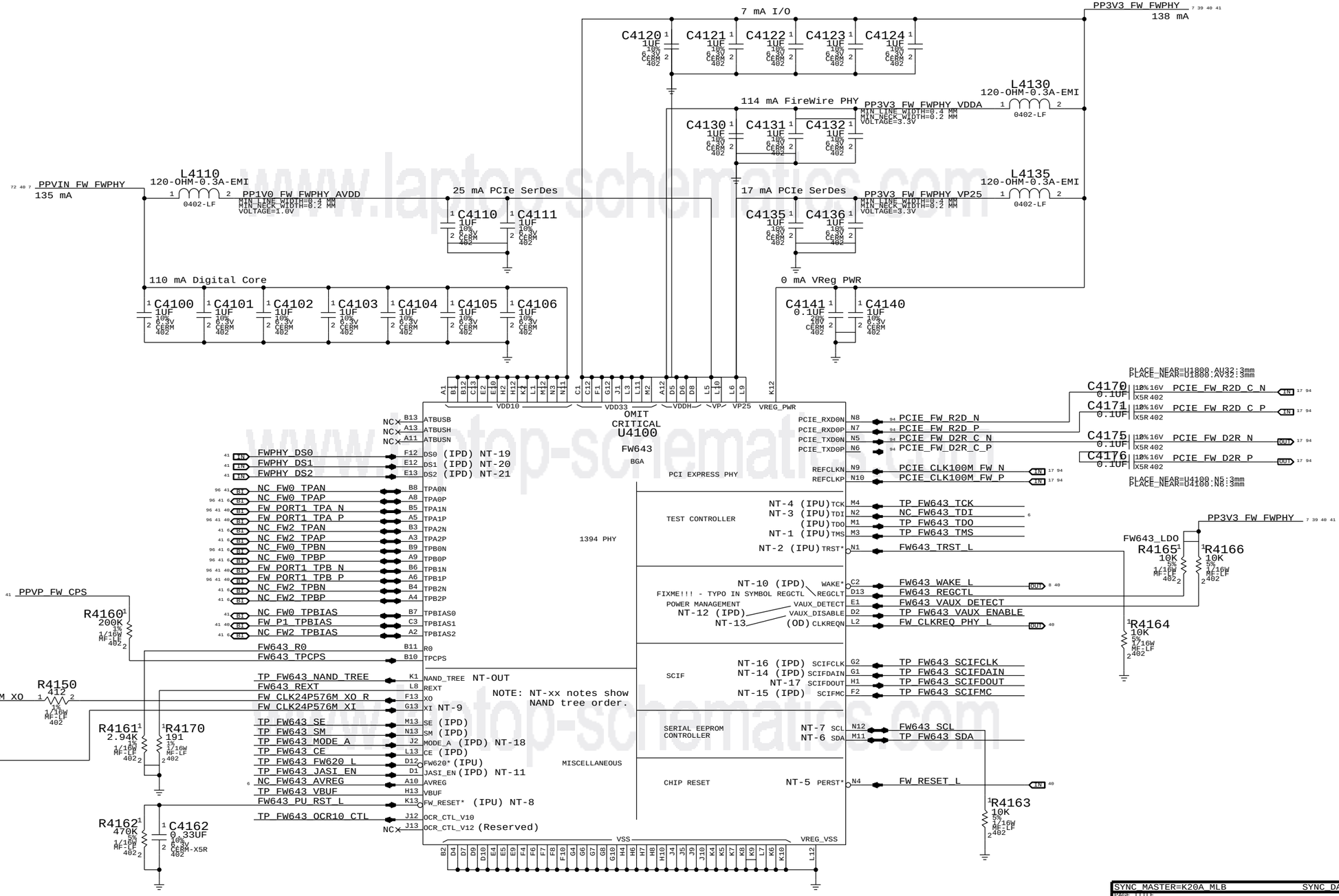

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

3.3V FW FET

I(max) = 1.7A (85C)

PP3V3_S0 → C4201 1UF 10% 6.3V X5R 402 → U4201 TPS22924 CSP (A2, B2, VIN, CRITICAL, ON, GND, C1, A1, VOUT, B1, C2) → PP3V3_FW_FWPHY

FW_PWR_EN → C2

1.05V FW FET

PPCPUVTT_S0 → C4202 1UF 10% 6.3V X5R 402 → U4202 TPS22924 CSP (A2, B2, VIN, CRITICAL, ON, GND, C1, A1, VOUT, B1, C2) → PP1V0_FW

FW_PWR_EN → C2

PP3V3_FW_FWPHY

R4277 10K 5% 1/16W MF-LF 402 (to PP3V3_FW_FWPHY)

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NOSTUFF C4276 0.1UF 10% 16V X5R 402

Q4276 DMB53D0UV SOT-563 (CRITICAL)

FW643_WAKE_L

FW_PLUG_DET_L

FW_CLKREQ_L

Q4261 SSM6N15FEAPE SOT563

FW_CLKREQ_PHY_L (IN) → FW_CLKREQ_PHY_L (OUT) MAKE_BASE=TRUE

FireWire Port Power Switch

PP3V3_S0 → R4281 100K 5% 1/16W MF-LF 402

R4280 10K 1% 1/16W MF-LF 402 (PPVIN_FW_FWPHY)

P1V0_FW_RC

C4281 1UF 10% 6.3V X5R 402

Q4299 DMB53D0UV SOT-563 (CRITICAL)

P1V0_RESET_GATE

R4283 10K 5% 1/16W MF-LF 402 → PLT_RESET_L (IN)

Q4299 DMB53D0UV SOT-563 (CRITICAL)

FW_RESET_L (OUT)

PP1V05_FW PGOOD/FW_RESET_L

Late-VG Protection

PP3V3_S0

C4200 0.1UF 10% 16V X5R 402 (PLACE_NEAR=U4200.1:4mm)

U4200 TPD4S1394 LLP (PLACE_NEAR=J4310.4:4mm)

- FW_PORT1_TPA_P (BI) → D1+
- FW_PORT1_TPA_N (BI) → D1-
- FW_PORT1_TPB_P (BI) → D2+
- FW_PORT1_TPB_N (BI) → D2-
- VCLMP → TP_FW_LATEVG_VCLMP
- FWPWR_EN
- GND

R4201 100K 5% 1/16W MF-LF 402

R4262 10K 5% 1/16W MF-LF 402 (PPBUS_G3H)

FWPWR_EN_TRI

R4263 10 5% 1/16W MF-LF 402

FWPWR_EN_TRI_R

Q4262 BSS8402DW SOT-363 (SYM-VER1)

R4260 470K 5% 1/16W MF-LF 402

C4260 0.1UF 10% 25V X5R 402

Q4260 NDS9407 SOI-HF (CRITICAL) → PPBUS_FW_FWBOOST

FWPWR_EN_L_DIV

R4261 330K 5% 1/16W MF-LF 402

FWPWR_EN_L

Q4261 SSM6N15FEAPE SOT563

NOSTUFF C4261 0.1UF 10% 16V X5R 402

PP10V_FW

F4260 1.5A-24V 1812L15024HF (CRITICAL)

PP10V_FW_D (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=10V)

D4260 SM CRS08-1.5A-30V (CRITICAL) → PPVP_FW

PPCPUVTT_S0

R4275 1K 5% 1/16W MF-LF 402 → FW_PWR_EN_L

Q4275 DMB53D0UV SOT-563 (CRITICAL) ← FW_PWR_EN

FW_P1_TPBIAS

R4270 330K 5% 1/16W MF-LF 402

Q4270 BC847CDXV6TXG SOT563 (CRITICAL)

FW_DET_MIRROR

R4272 1K 5% 1/16W MF-LF 402

FW_P1_TPBIAS_R

PLACE_NEAR=C4360.1:4mm

R4271 56K 5% 1/16W MF-LF 402

Q4270 BC847CDXV6TXG SOT563

FW_DET_EMIT

R4273 12K 5% 1/16W MF-LF 402

FW_PLUG_DET

C4270 0.1UF 10% 16V X5R 402

Q4275 DMB53D0UV SOT-563 (CRITICAL) → FW_PLUG_DET_L (OUT)

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: FireWire Port Power

Apple Inc.

DRAWING NUMBER: SIZE D

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

41 40 39 7 PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

41 39 FWPHY_DS0 — FWPHY_DS0 39 41 (MAKE_BASE=TRUE)

41 39 FWPHY_DS2 — FWPHY_DS2 39 41 (MAKE_BASE=TRUE)

41 39 FWPHY_DS1 — FWPHY_DS1 39 41 (MAKE_BASE=TRUE)

R4381 10K 1% 1/10W MF-LF 402

41 39 NC_FW0_TPBIAS — NC_FW0_TPBIAS 39 41 (MAKE_BASE=TRUE)

41 39 6 NC_FW2_TPBIAS — NC_FW2_TPBIAS 6 39 41 (MAKE_BASE=TRUE)

96 41 39 NC_FW0_TPAN — NC_FW0_TPAN 39 41 96 (MAKE_BASE=TRUE)

96 41 39 6 NC_FW0_TPAP — NC_FW0_TPAP 6 39 41 96 (MAKE_BASE=TRUE)

41 39 6 NC_FW2_TPAN — NC_FW2_TPAN 6 39 41 (MAKE_BASE=TRUE)

41 39 6 NC_FW2_TPAP — NC_FW2_TPAP 6 39 41 (MAKE_BASE=TRUE)

96 41 39 6 NC_FW0_TPBN — NC_FW0_TPBN 6 39 41 96 (MAKE_BASE=TRUE)

96 41 39 6 NC_FW0_TPBP — NC_FW0_TPBP 6 39 41 96 (MAKE_BASE=TRUE)

41 39 6 NC_FW2_TPBN — NC_FW2_TPBN 6 39 41 (MAKE_BASE=TRUE)

41 39 6 NC_FW2_TPBP — NC_FW2_TPBP 6 39 41 (MAKE_BASE=TRUE)

Termination

Place close to FireWire PHY

40 39 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.A5:2mm

PLACE_NEAR=U4100.B5:2mm

96 41 40 39 FW_PORT1_TPA_P — FW_PORT1_TPA_P 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPA_N — FW_PORT1_TPA_N 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPB_P — FW_PORT1_TPB_P 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPB_N — FW_PORT1_TPB_N 39 40 41 96 (MAKE_BASE=TRUE)

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.B6:4mm

PLACE_NEAR=U4100.A6:4mm

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

41 40 7 6 PPVP_FW

R4311 470K 5% 1/16W MF-LF 402

Q4300 BSS84Q2DW SOT-363 (SYM-VER1)

41 39 PPVP_FW_CPS — PPVP_FW_CPS 39 41 (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=12.6V)

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

41 40 39 7 PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

41 40 7 6 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F (MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=33V)

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

OUTPUT

INPUT

CHASSIS GND

514S0605

96 41 40 39 FW_PORT1_TPB_N — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPB_P — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPA_N — ESD_HOT=TRUE

96 41 40 39 FW_PORT1_TPA_P — ESD_HOT=TRUE

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

C4319 0.1uF 10% 50V X7R 603-1

PLACE_NEAR=J4310.5:3mm

R4319 1M 5% 1/16W MF-LF 402

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=K18_MLB SYNC_DATE=07/08/2009

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: SIZE D

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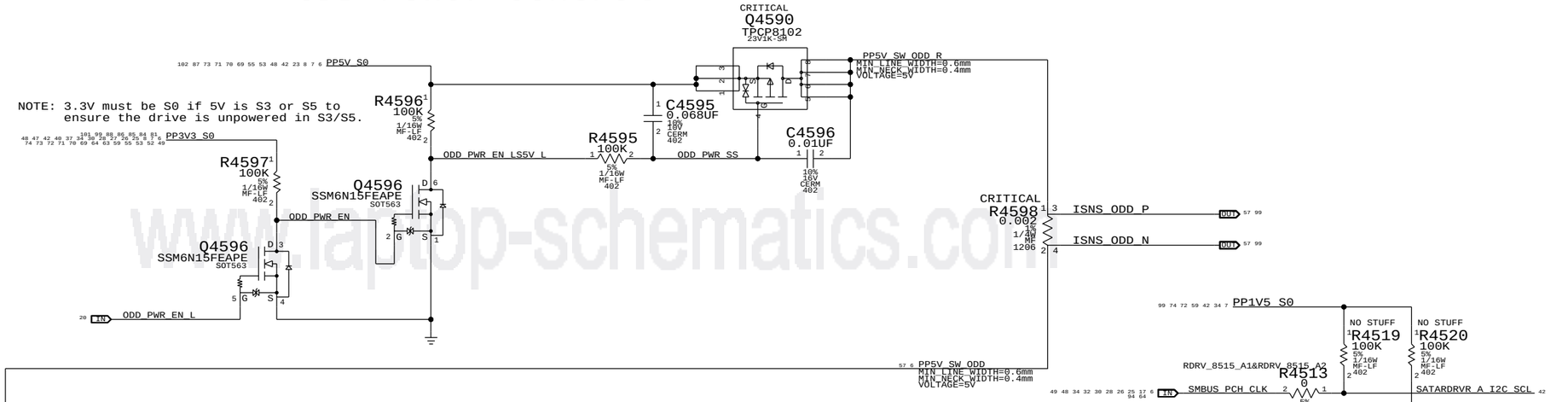
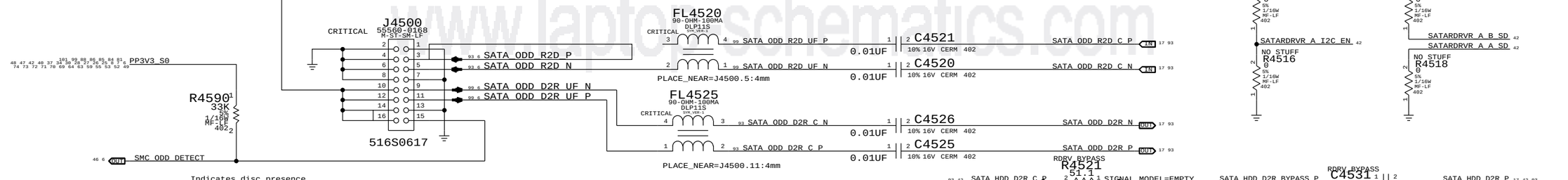
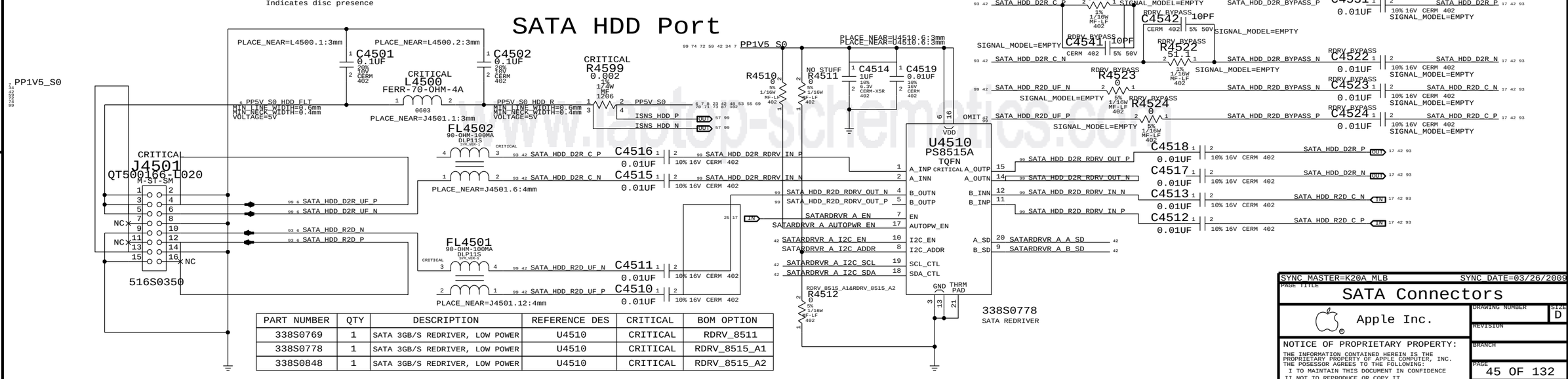
ODD Power Control



SATA ODD Port



SATA HDD Port



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A1
338S0848	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A2

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: D

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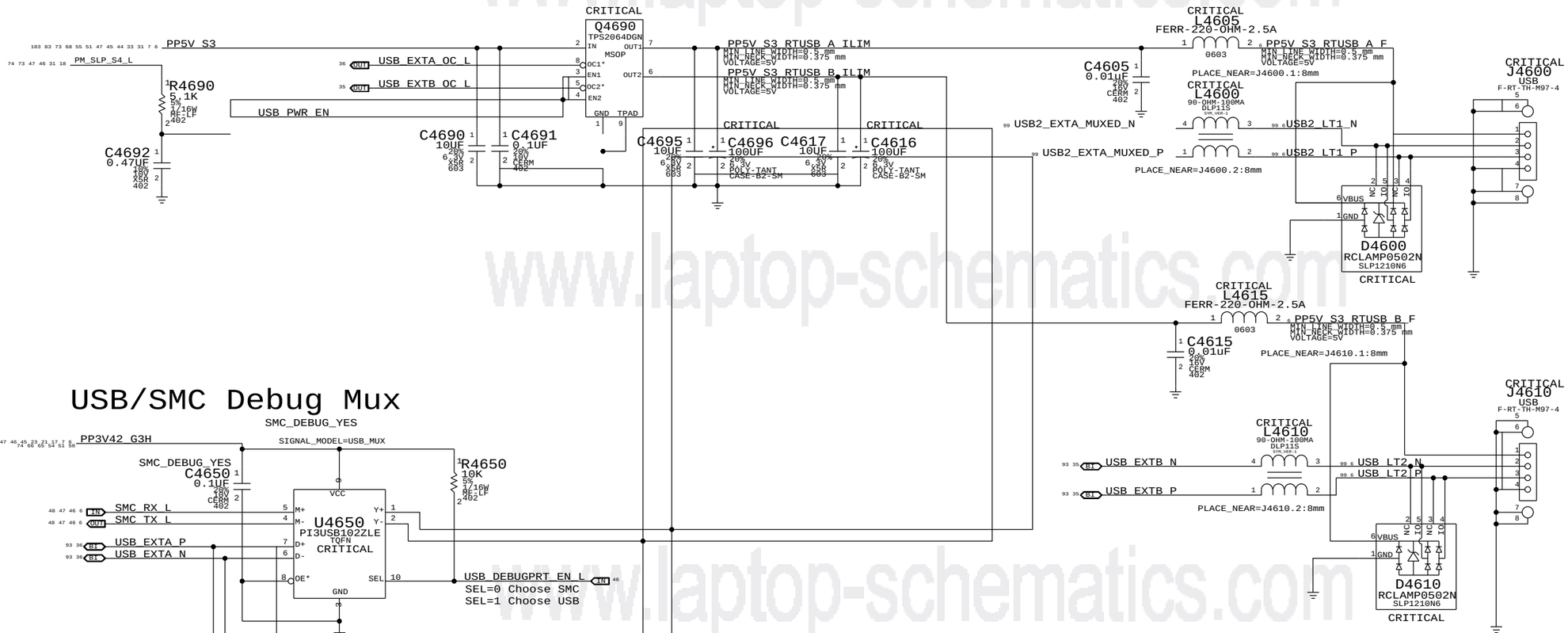
Port Power Switch



Left USB Port A

USB/SMC Debug Mux

Left USB Port B

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: External USB Connectors

Apple Inc.

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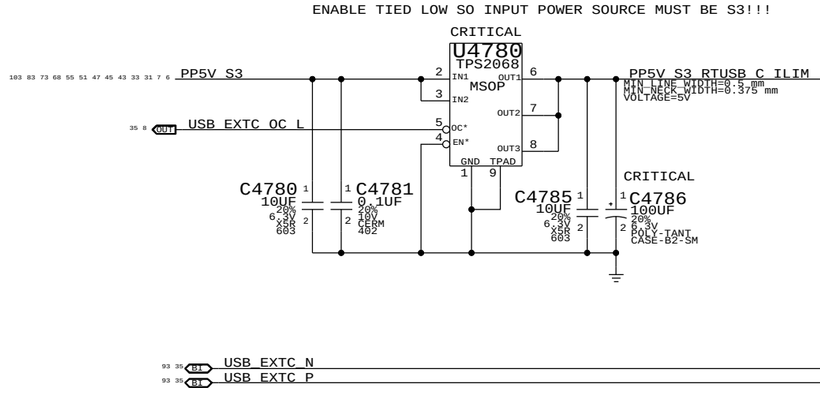
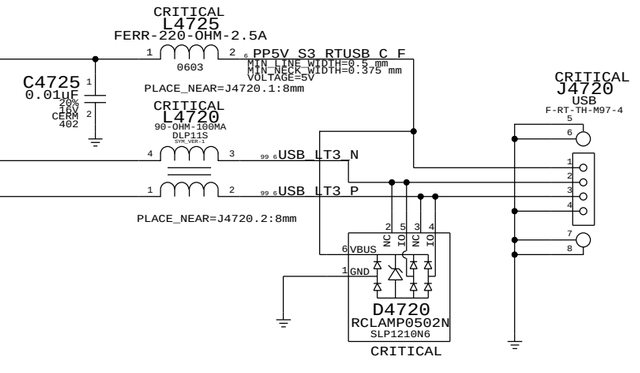
Port Power Switch

ENABLE TIED LOW SO INPUT POWER SOURCE MUST BE S3!!!



LEFT USB PORT C



DRAWING NUMBER — SIZE D

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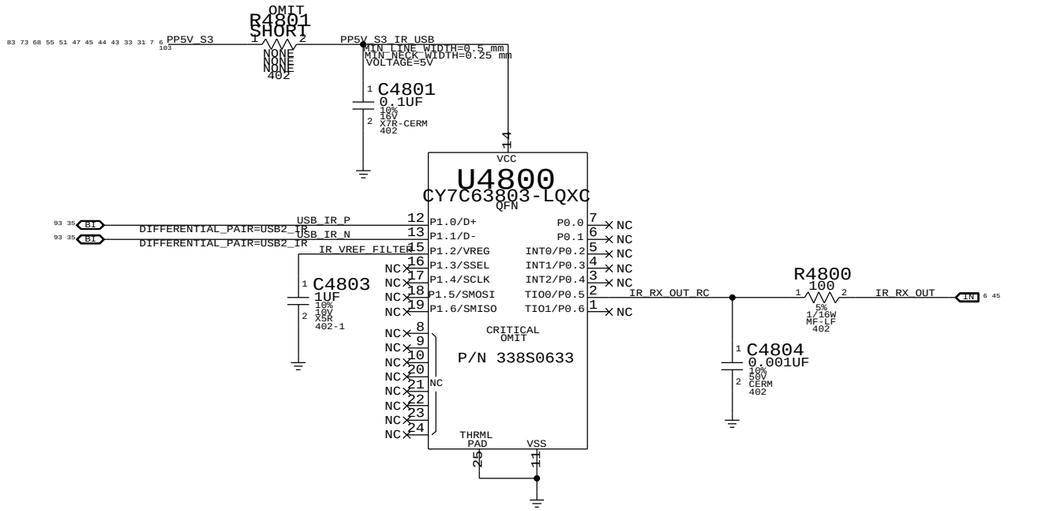
SHEET 44 OF 103



SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: Front Flex Support

Apple Inc.

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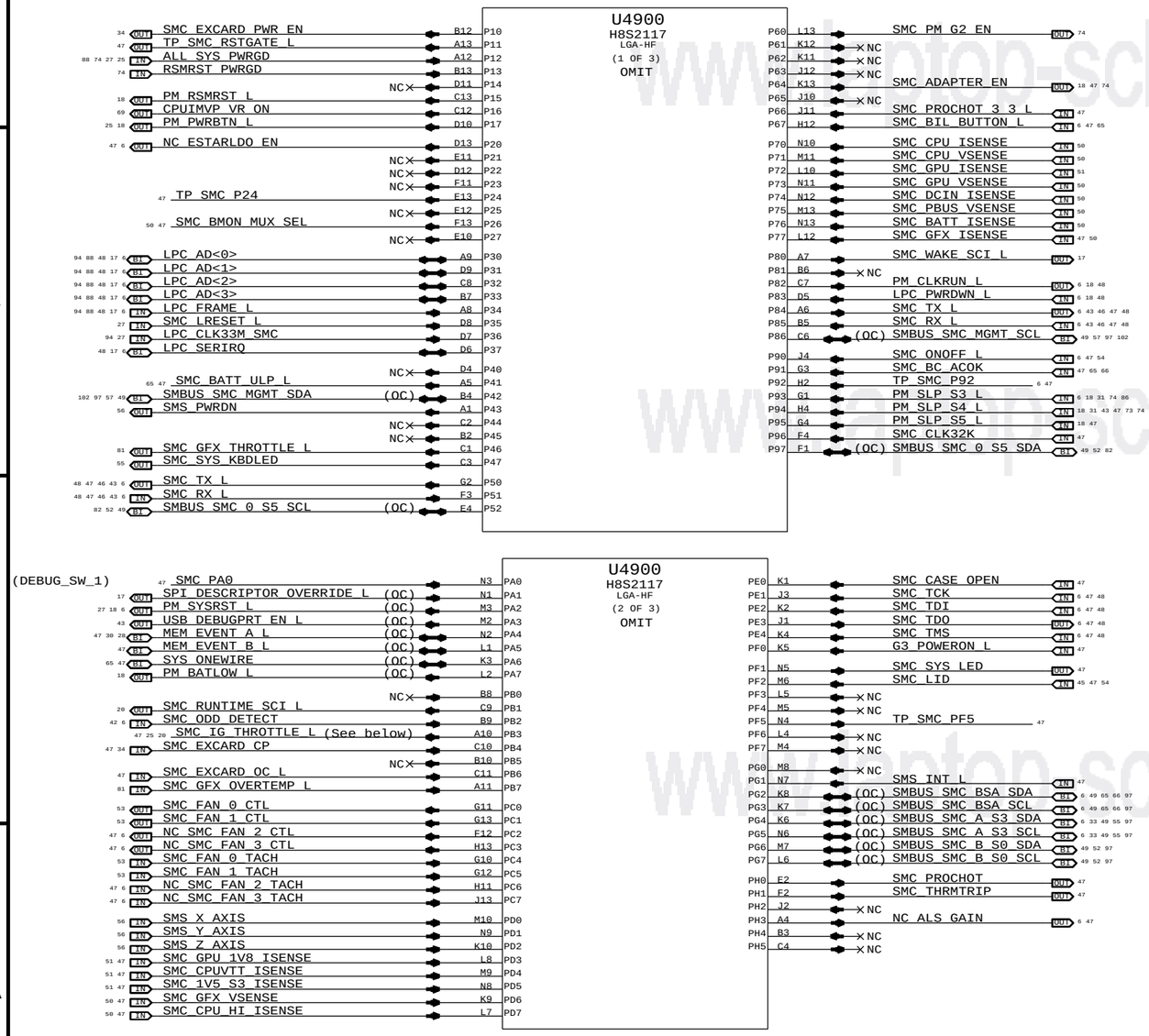
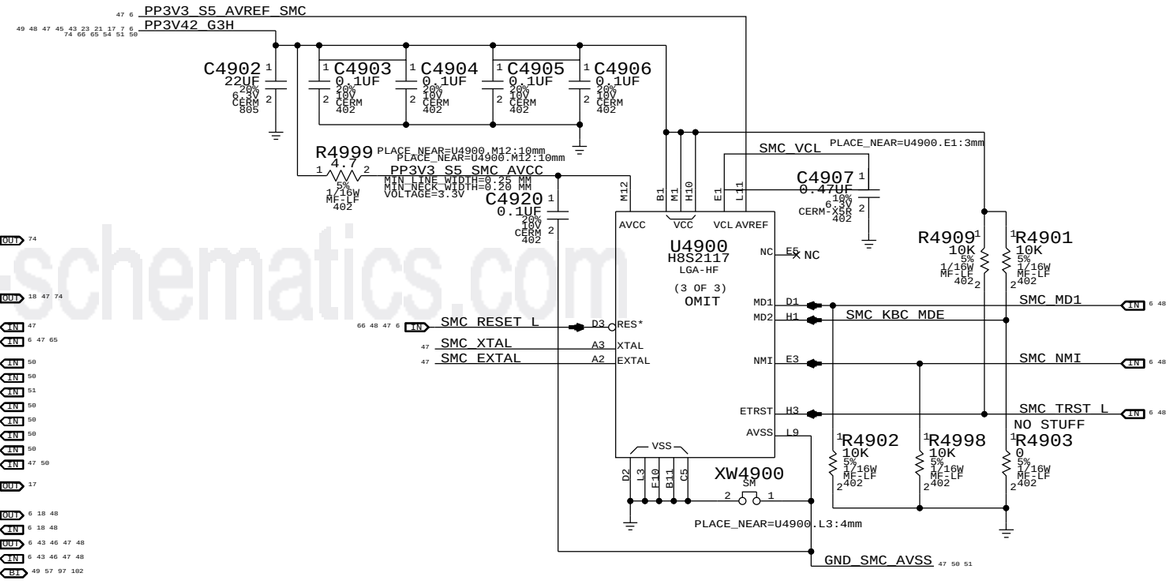
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER | SIZE: D

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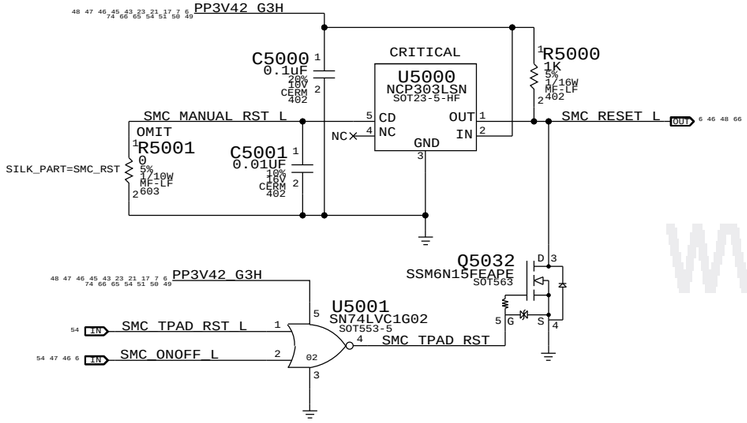
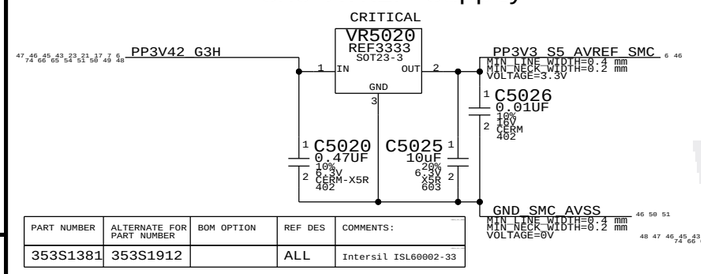
SMC Reset "Button" / Brownout Detect

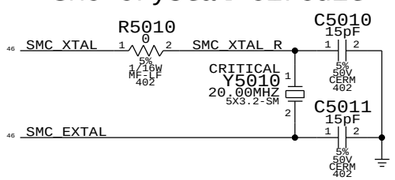


SMC AVREF Supply

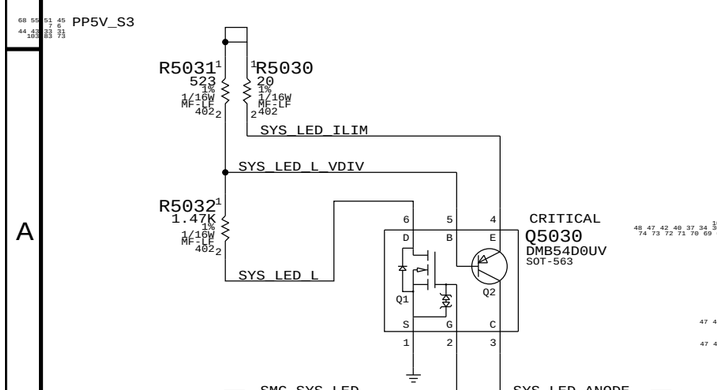


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

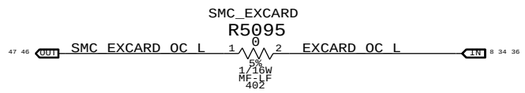
SMC Crystal Circuit



System (Sleep) LED Circuit

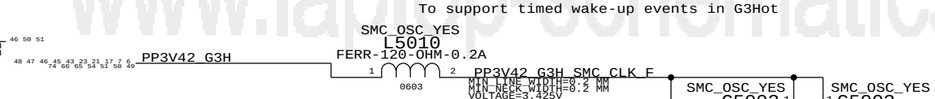


SMC_EXCARD

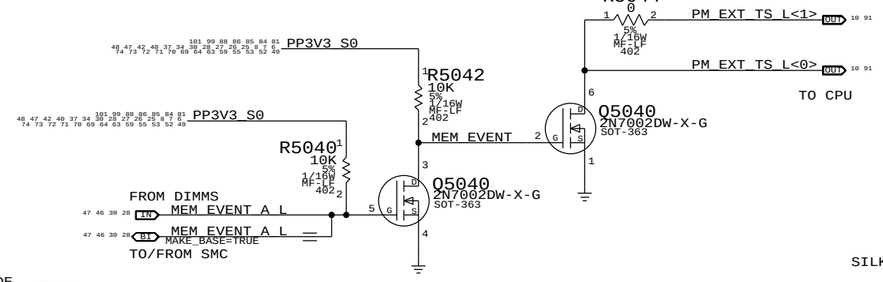


SMC G3Hot 32kHz Oscillator

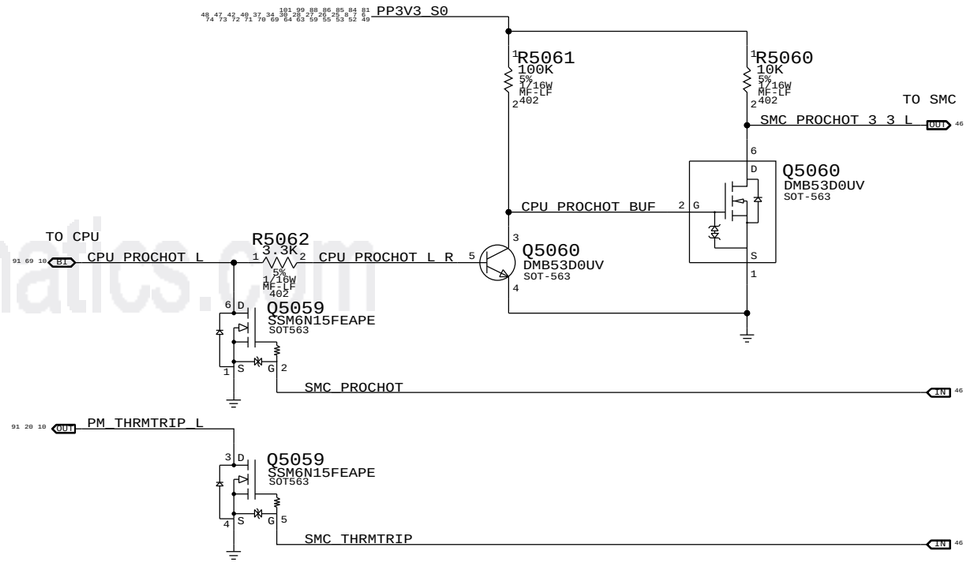
To support timed wake-up events in G3Hot



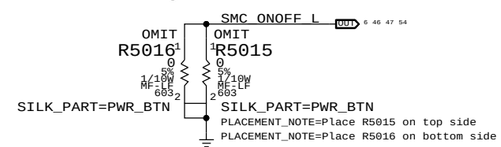
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting

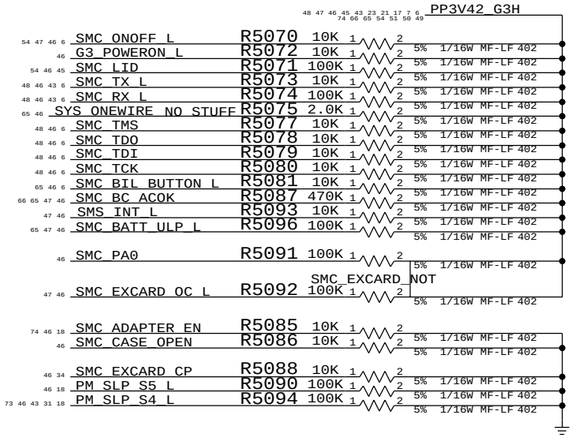


SMC FSB to 3.3V Level Shifting



Debug Power "Buttons"





SYNC_MASTER=K17_REF	SYNC_DATE=06/17/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER: — SIZE: D
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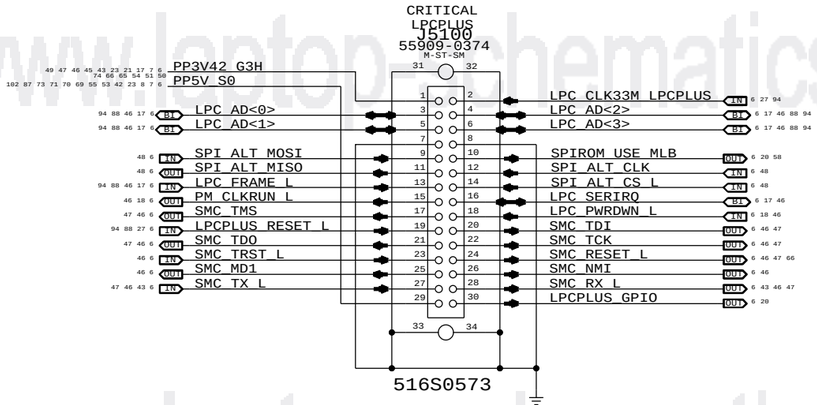
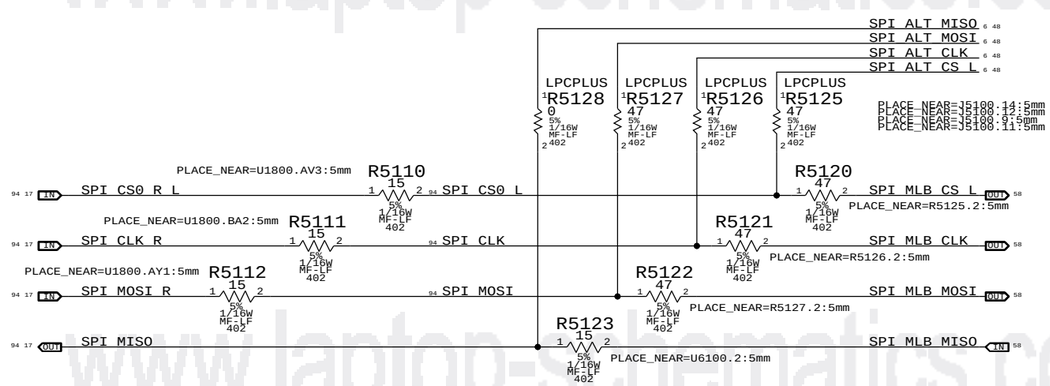
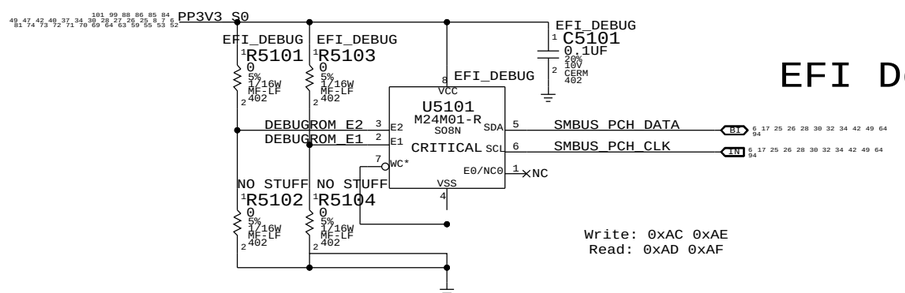
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=T22_MLB SYNC_DATE=03/30/2009

PAGE TITLE: LPC+SPI Debug Connector

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 1% 1/16W MF-LF 402
R5201 1K 1% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA
MAKE_BASE=TRUE

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs
U2900
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC 0xAE)
(Read: 0xAD 0xAF)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

ExpressCard Slot
J3500
(Address via ARP)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDD Re-driver Control
U4510
(Write: 0x94 Read: 0x95)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)
- SML_PCH_0_CLK
- SML_PCH_0_DATA
MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402
R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)
- SML_PCH_1_CLK
- SML_PCH_1_DATA
MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA
MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414: U5550
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)
- SMBUS_SMC_0_S5_SCL
- SMBUS_SMC_0_S5_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

CPU Temp
EMC1414: U5570
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 2.0K 5% 1/16W MF-LF 402
R5281 2.0K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S5

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

Sensor ADC B
UC210
(Write: 0x32 Read: 0x33)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

SYNC_MASTER=K17_WFERRY SYNC_DATE=05/20/2009

PAGE TITLE
K17 SMBus Connections

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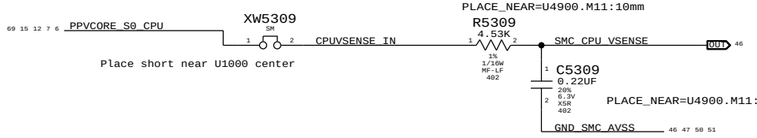
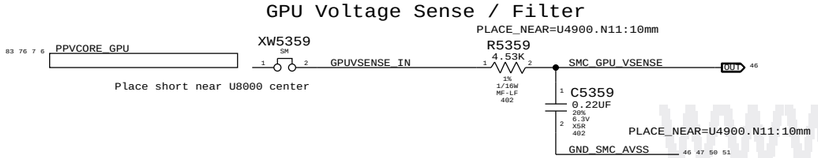
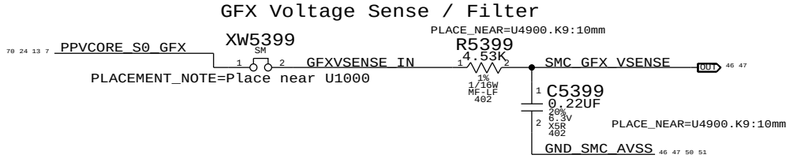
CPU Voltage Sense / Filter



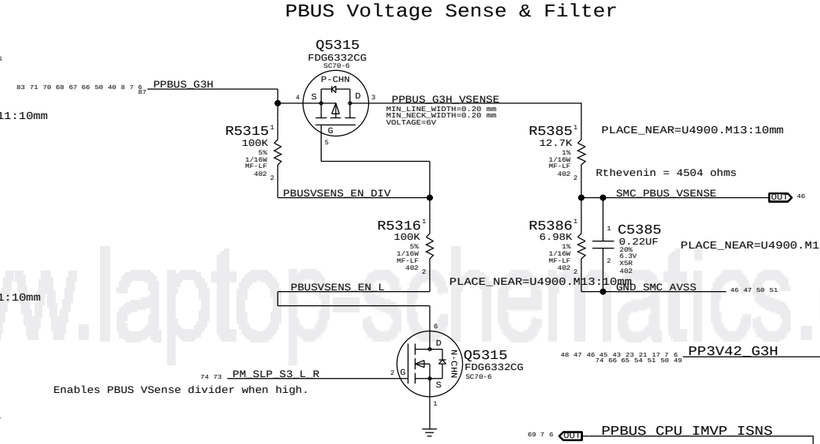
GPU Voltage Sense / Filter



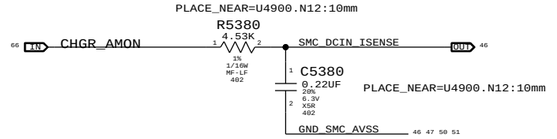
GFX Voltage Sense / Filter



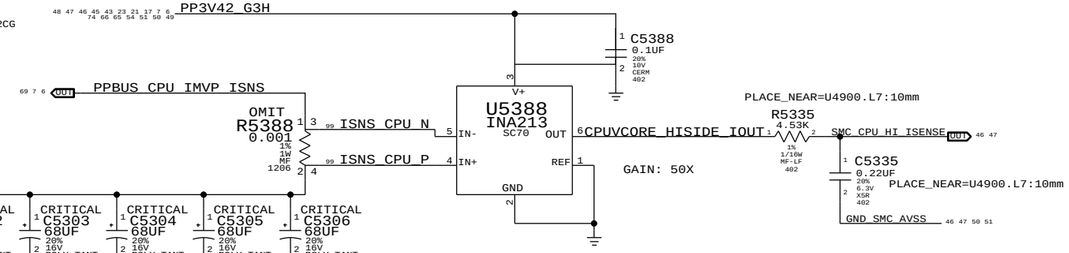
PBUS Voltage Sense & Filter



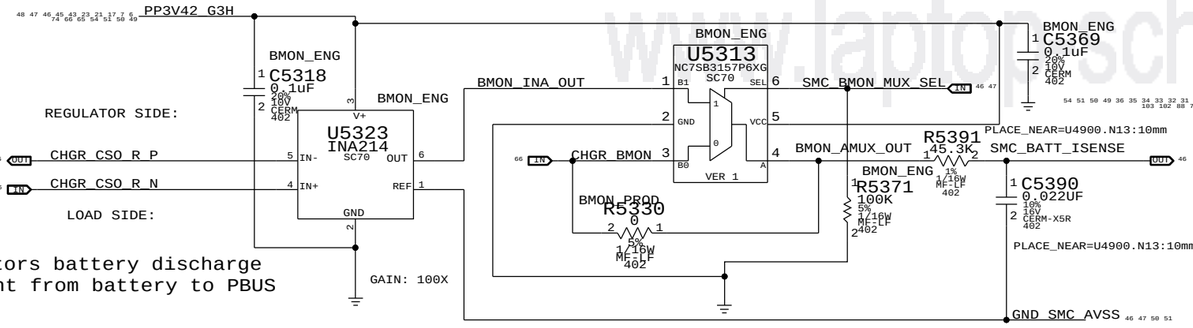
DCIN Current Sense Filter



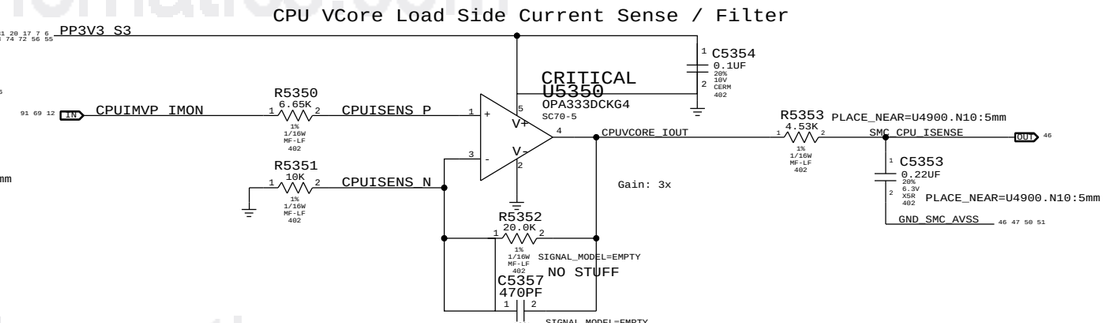
CPU VCore High Side Current Sensor



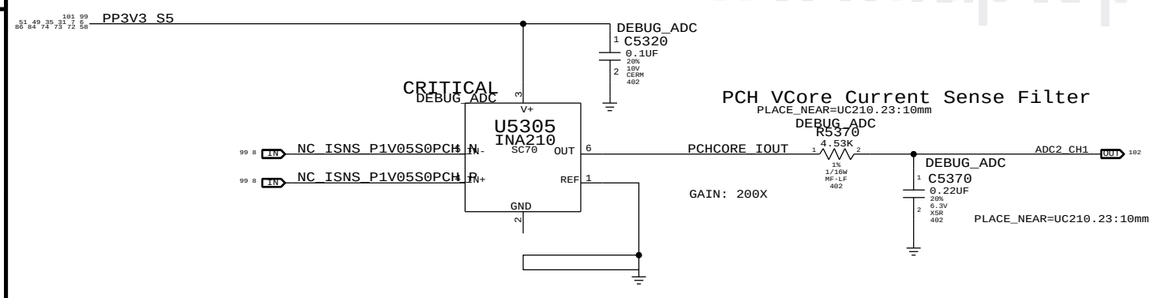
BMON Current Sense - Entire circuit must be near SMC (U4900)



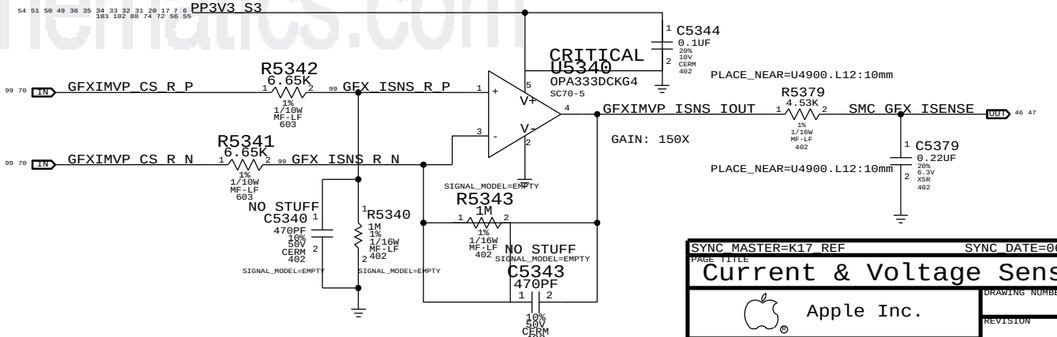
CPU VCore Load Side Current Sense / Filter



PCH VCore Current Sense



GFX/AXG Current Sense



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
102S0858	1	RES,1/2W,1%,0.010 OHM,SMD	R5388		

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

PAGE TITLE

Current & Voltage Sensing

Apple Inc.

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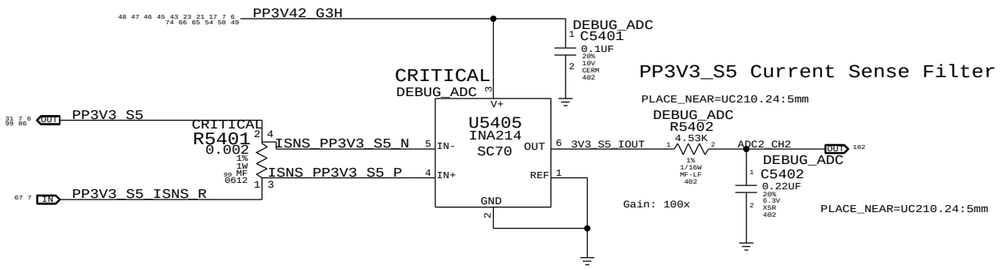
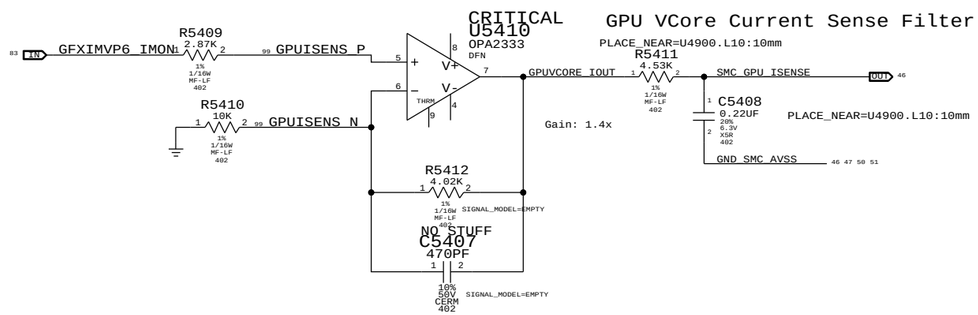
PP3V3_S5 Current Sense

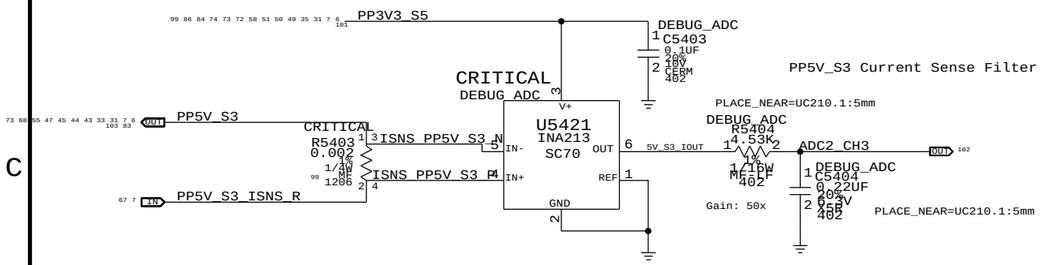


GPU VCore Current Sense

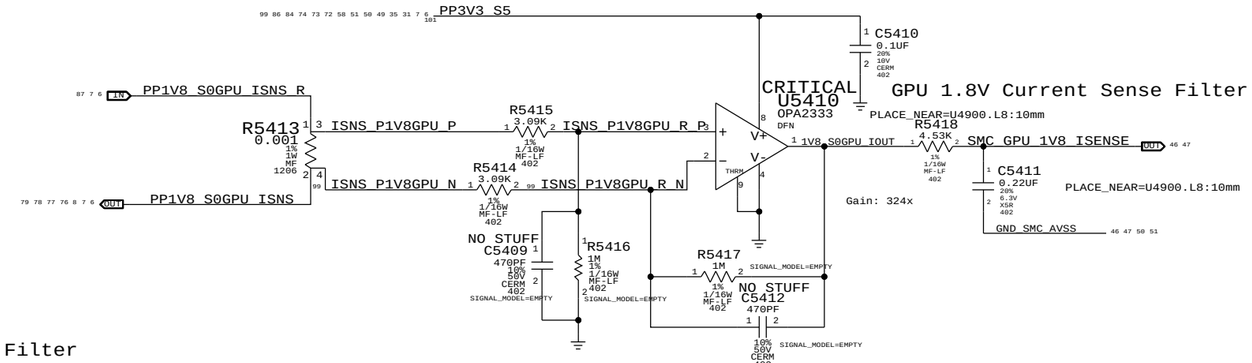


GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

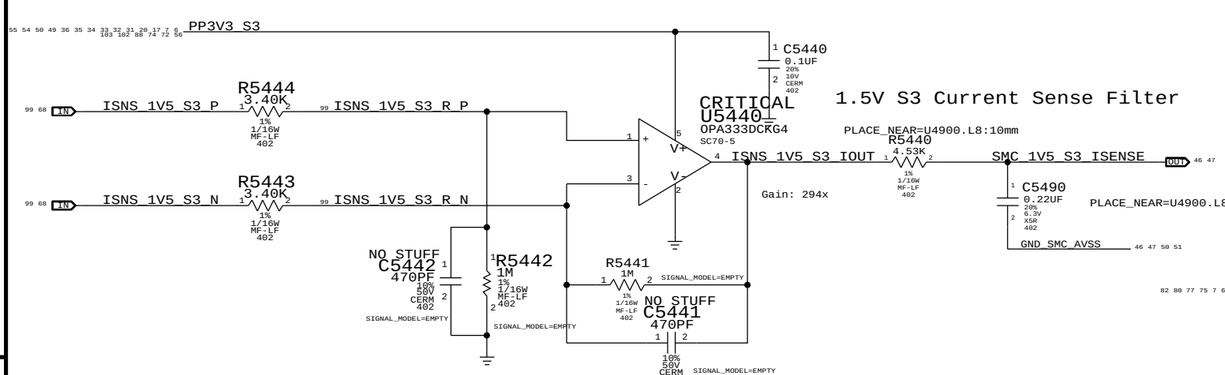
PP5V_S3 Current Sense



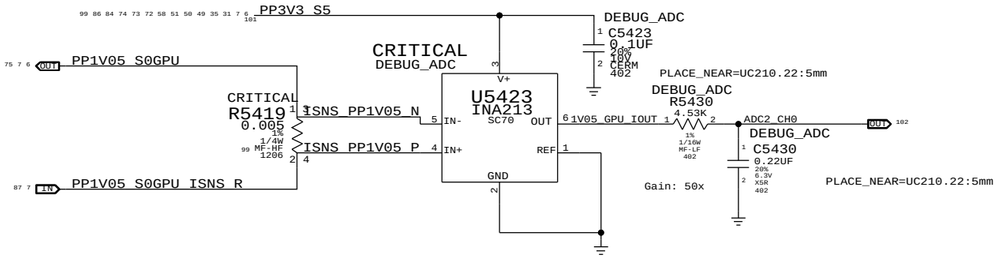
GPU 1.8V Current Sense



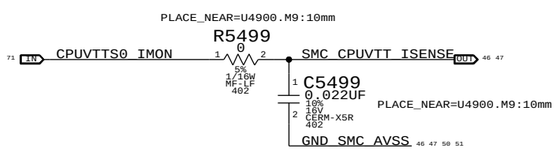
1.5V S3 Current Sense



GPU 1.05V Current Sense



CPUVTT 1.05V Current Sense



SYNC_MASTER=K17_CHENGD SYNC_DATE=06/04/2009

PAGE TITLE

Current Sensing

Apple Inc.

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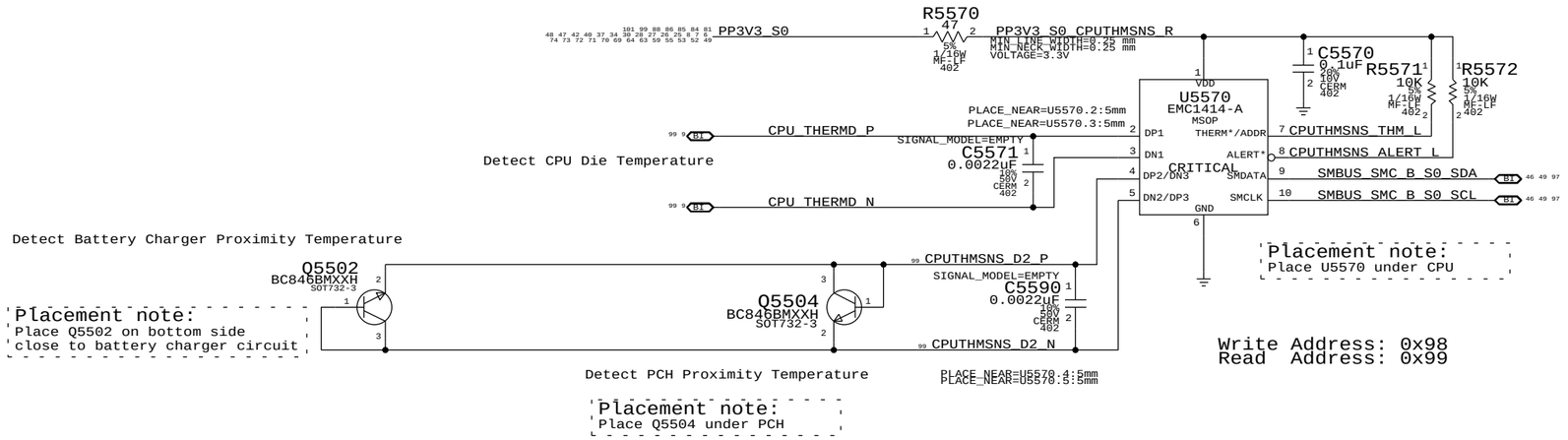
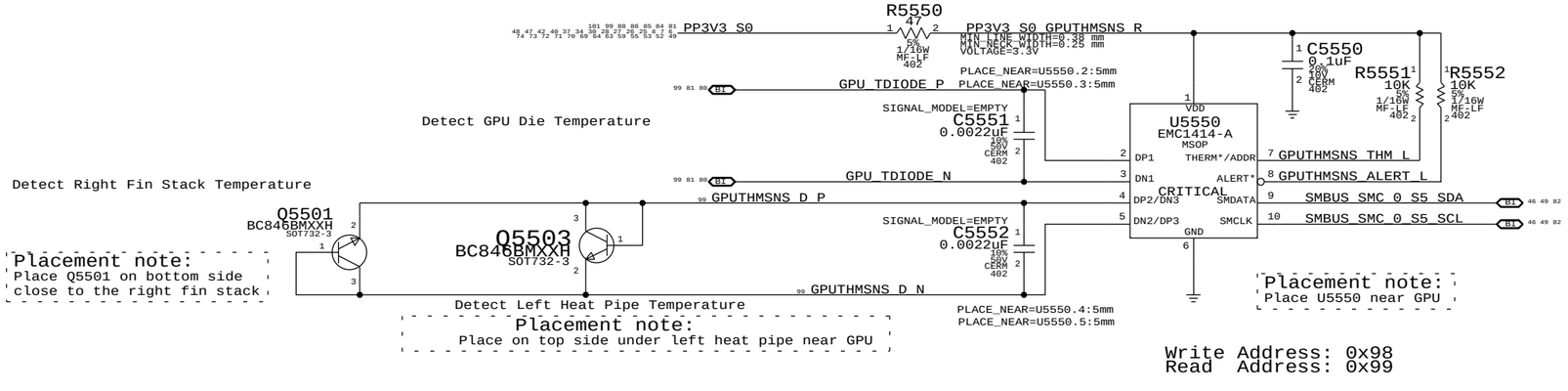
CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



SYNC_MASTER=K17_CHENGD SYNC_DATE=07/08/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

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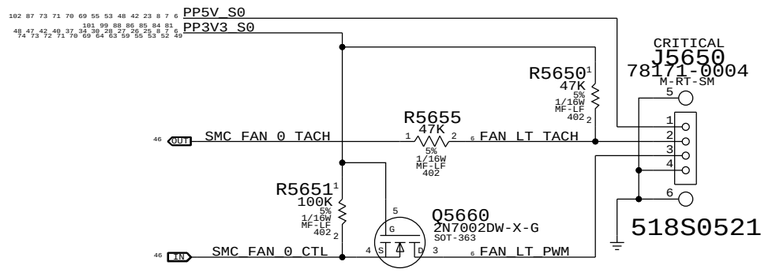
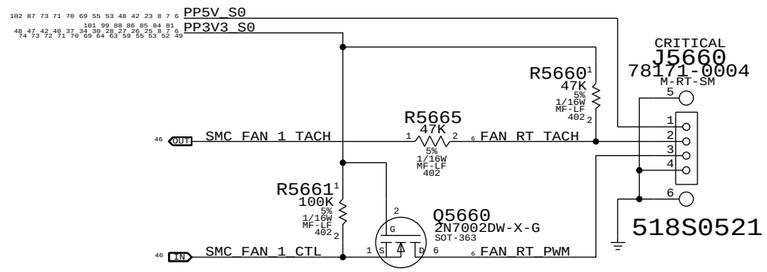
Left Fan



Right Fan



SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE

Fan Connectors

Apple Inc.

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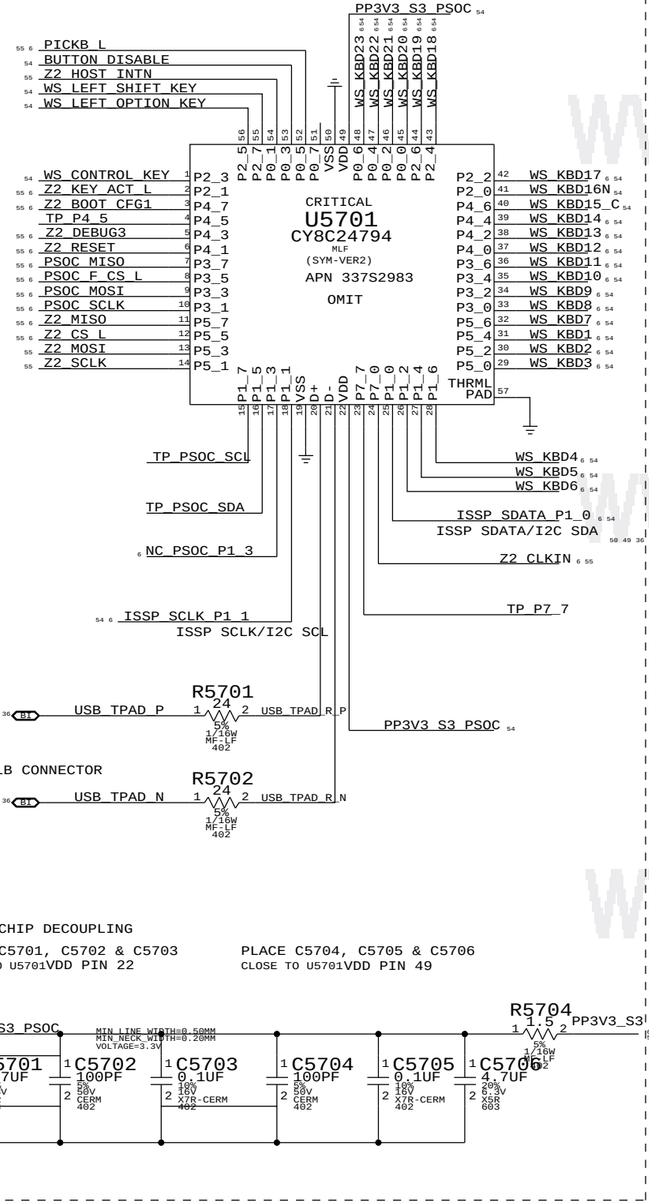
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

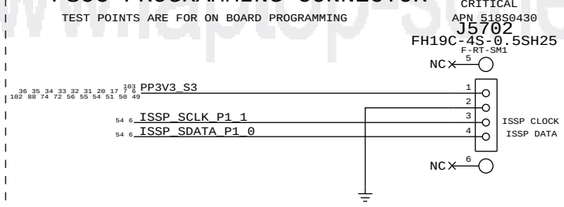
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

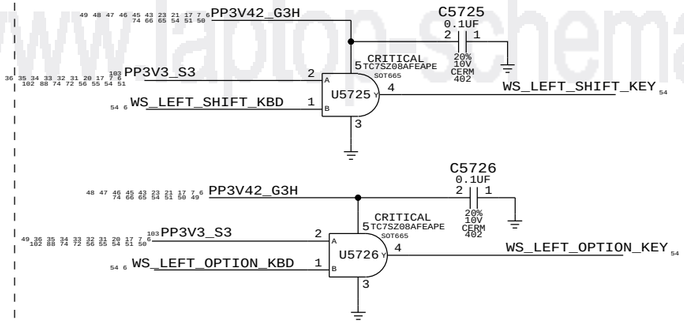
PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

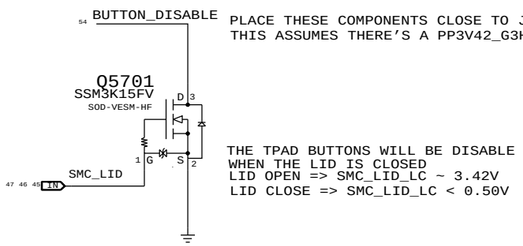


TPAD_DEBUG
CRITICAL
APN 518S0430

ISOLATION CIRCUIT



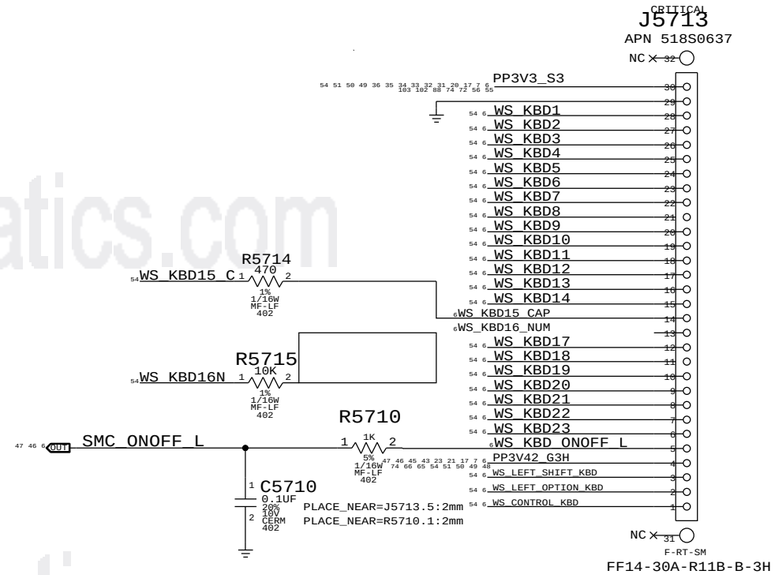
TPAD BUTTONS DISABLE



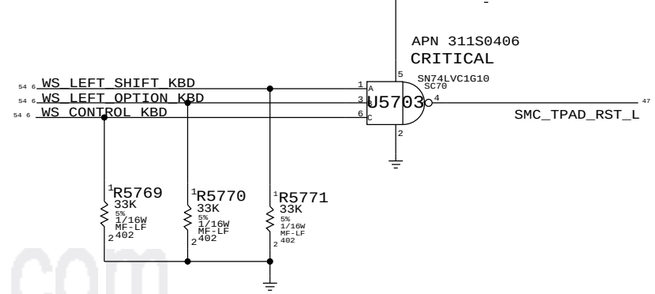
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER: D
SIZE: D
REVISION:
BRANCH:
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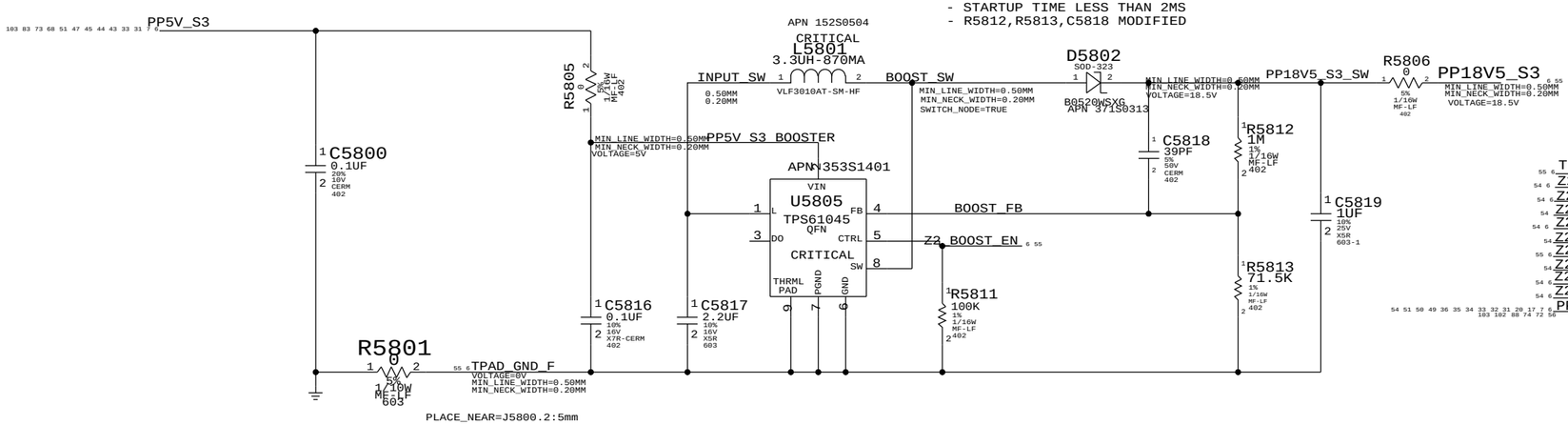
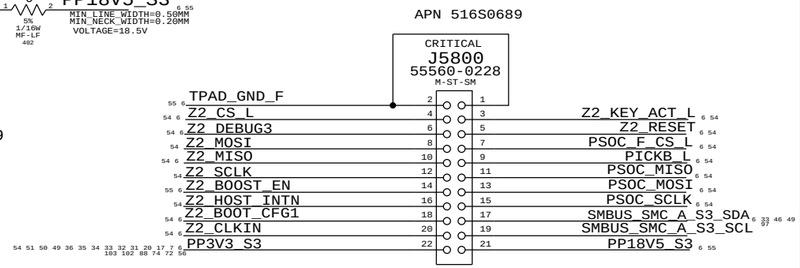
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



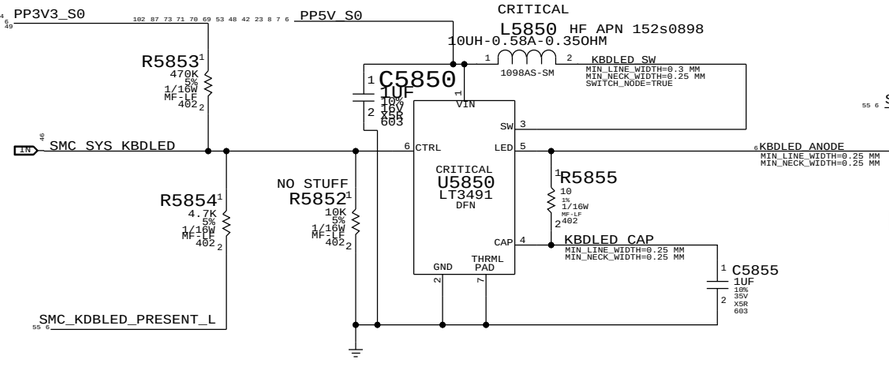
IPD FLEX CONNECTOR



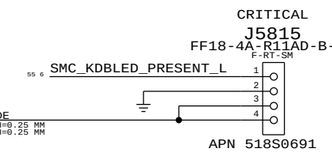
Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT



KBD BACKLIGHT CONNECTOR



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

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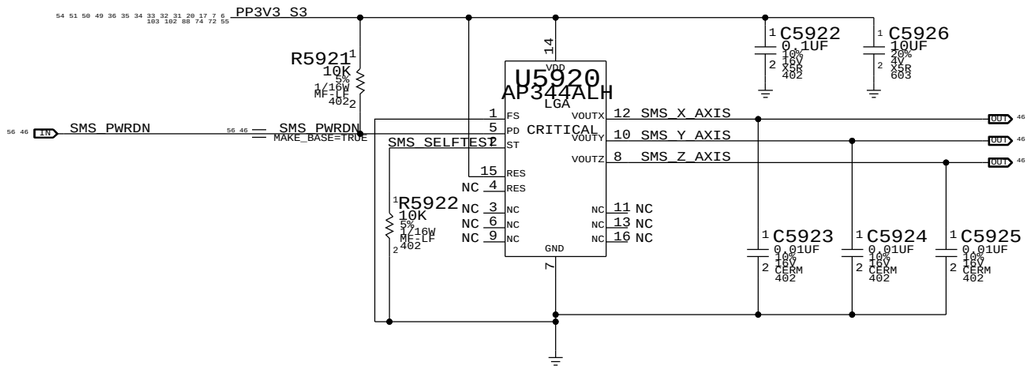
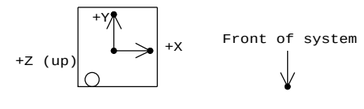
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE
Sudden Motion Sensor (SMS)

Apple Inc.

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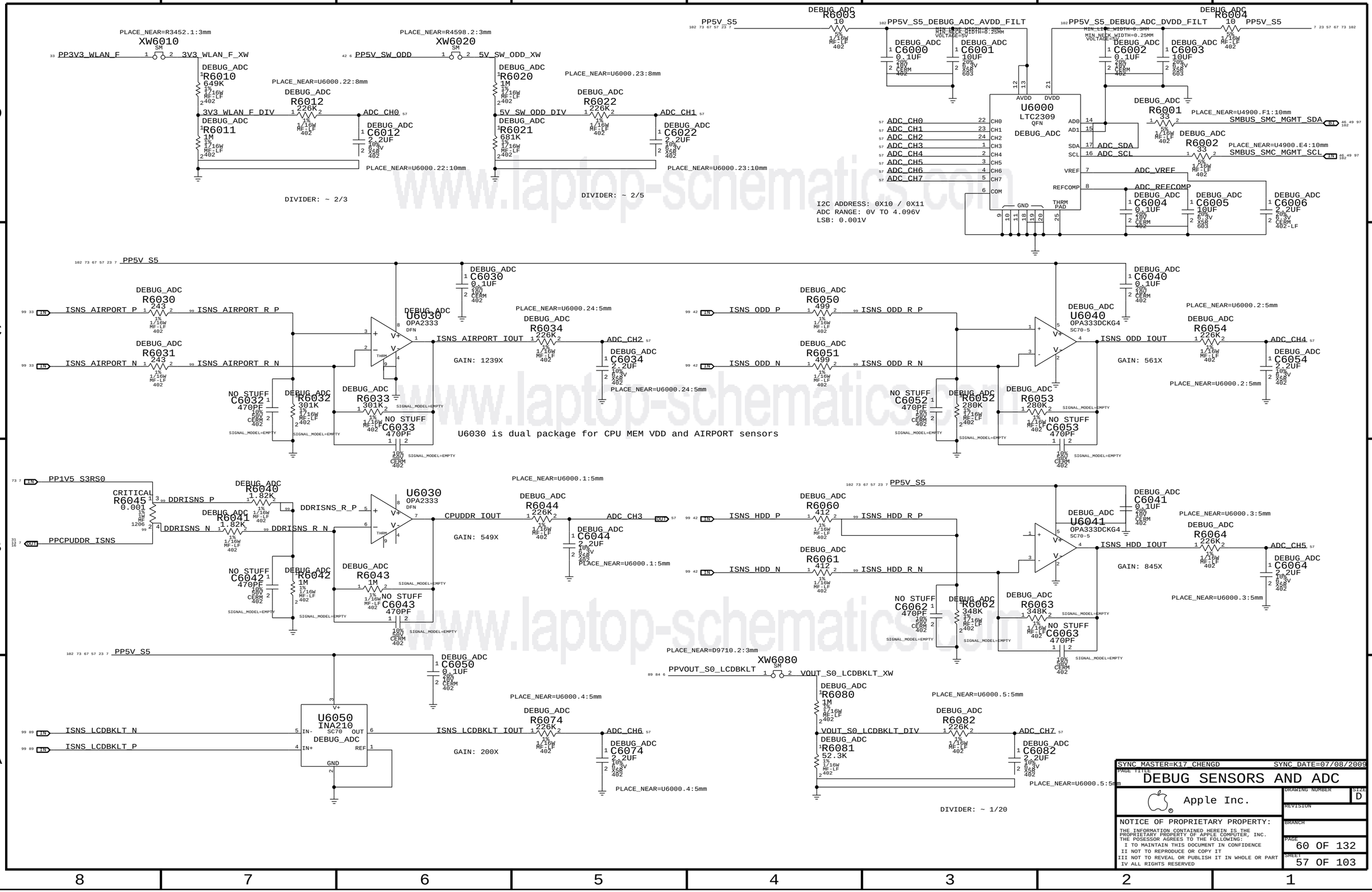
PLACE_NEAR=R3452.1:3mm
XW6010
PP3V3_WLAN_F
3V3_WLAN_F_XW
R6010 649K
R6011 1M
3V3_WLAN_F_DIV
R6012 226K
ADC_CH0
C6012 2.2UF
PLACE_NEAR=U6000.22:8mm
PLACE_NEAR=U6000.22:10mm
DIVIDER: ~ 2/3
PLACE_NEAR=R4598.2:3mm
XW6020
PP5V_SW_ODD
5V_SW_ODD_XW
R6020 1M
R6021 681K
5V_SW_ODD_DIV
R6022 226K
ADC_CH1
C6022 2.2UF
PLACE_NEAR=U6000.23:8mm
PLACE_NEAR=U6000.23:10mm
DIVIDER: ~ 2/5
PP5V_S5
R6003 10
PP5V_S5_DEBUG_ADC_AVDD_FILT
PP5V_S5_DEBUG_ADC_DVDD_FILT
R6004 10
C6000 0.1UF
C6001 10UF
C6002 0.1UF
C6003 10UF
U6000 LTC2309 QFN
AVDD
DVDD
GND
THRM PAD
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
COM
R6001 33
SMBUS_SMC_MGMT_SDA
R6002 33
SMBUS_SMC_MGMT_SCL
ADC_SDA
ADC_SCL
ADC_VREF
ADC_REFCOMP
C6004 0.1UF
C6005 10UF
C6006 2.2UF
I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V
PP5V_S5
R6030 243
ISNS_AIRPORT_P
R6031 243
ISNS_AIRPORT_N
U6030 OPA2333 DFN
C6030 0.1UF
R6034 226K
ISNS_AIRPORT_IOUT
ADC_CH2
C6034 2.2UF
GAIN: 1239X
PLACE_NEAR=U6000.24:5mm
R6032 301K
R6033 301K
C6032 470PF
C6033 470PF
NO STUFF
U6030 is dual package for CPU MEM VDD and AIRPORT sensors
R6050 499
ISNS_ODD_P
R6051 499
ISNS_ODD_N
U6040 OPA333DCKG4 SC70-5
C6040 0.1UF
R6054 226K
ISNS_ODD_IOUT
ADC_CH4
C6054 2.2UF
GAIN: 561X
PLACE_NEAR=U6000.2:5mm
R6052 280K
R6053 280K
C6052 470PF
C6053 470PF
PP1V5_S3RS0
CRITICAL
R6045 0.001 1W 1206
DDRISNS_P
DDRISNS_N
PPCPUDDR_ISNS
R6040 1.82K
R6041 1.82K
R6042 1M
R6043 1M
C6042 470PF
C6043 470PF
U6030 OPA2333 DFN
DDRISNS_R_P
DDRISNS_R_N
CPUDDR_IOUT
R6044 226K
ADC_CH3
C6044 2.2UF
GAIN: 549X
PLACE_NEAR=U6000.1:5mm
R6060 412
ISNS_HDD_P
R6061 412
ISNS_HDD_N
U6041 OPA333DCKG4 SC70-5
C6041 0.1UF
R6064 226K
ISNS_HDD_IOUT
ADC_CH5
C6064 2.2UF
GAIN: 845X
PLACE_NEAR=U6000.3:5mm
R6062 348K
R6063 348K
C6062 470PF
C6063 470PF
PP5V_S5
C6050 0.1UF
U6050 INA210 SC70
ISNS_LCDBKLT_N
ISNS_LCDBKLT_P
R6074 226K
ISNS_LCDBKLT_IOUT
ADC_CH6
C6074 2.2UF
GAIN: 200X
PLACE_NEAR=U6000.4:5mm
PLACE_NEAR=D9710.2:3mm
XW6080
PPVOUT_S0_LCDBKLT
VOUT_S0_LCDBKLT_XW
R6080 1M
VOUT_S0_LCDBKLT_DIV
R6081 52.3K
R6082 226K
ADC_CH7
C6082 2.2UF
PLACE_NEAR=U6000.5:5mm
DIVIDER: ~ 1/20
SYNC_MASTER=K17 CHENGD
SYNC_DATE=07/08/2009
PAGE TITLE
DEBUG SENSORS AND ADC
Apple Inc.
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SIZE D
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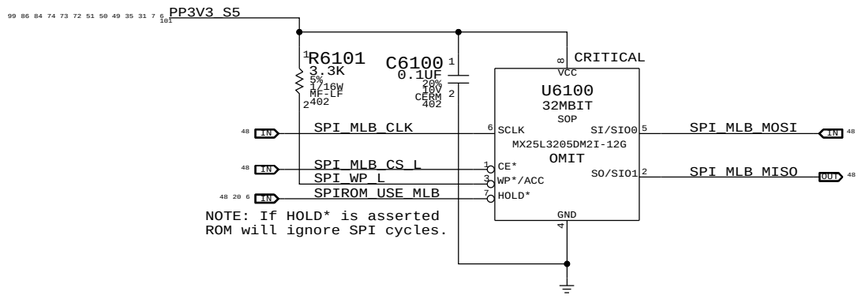

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE

SPI ROM

Apple Inc.

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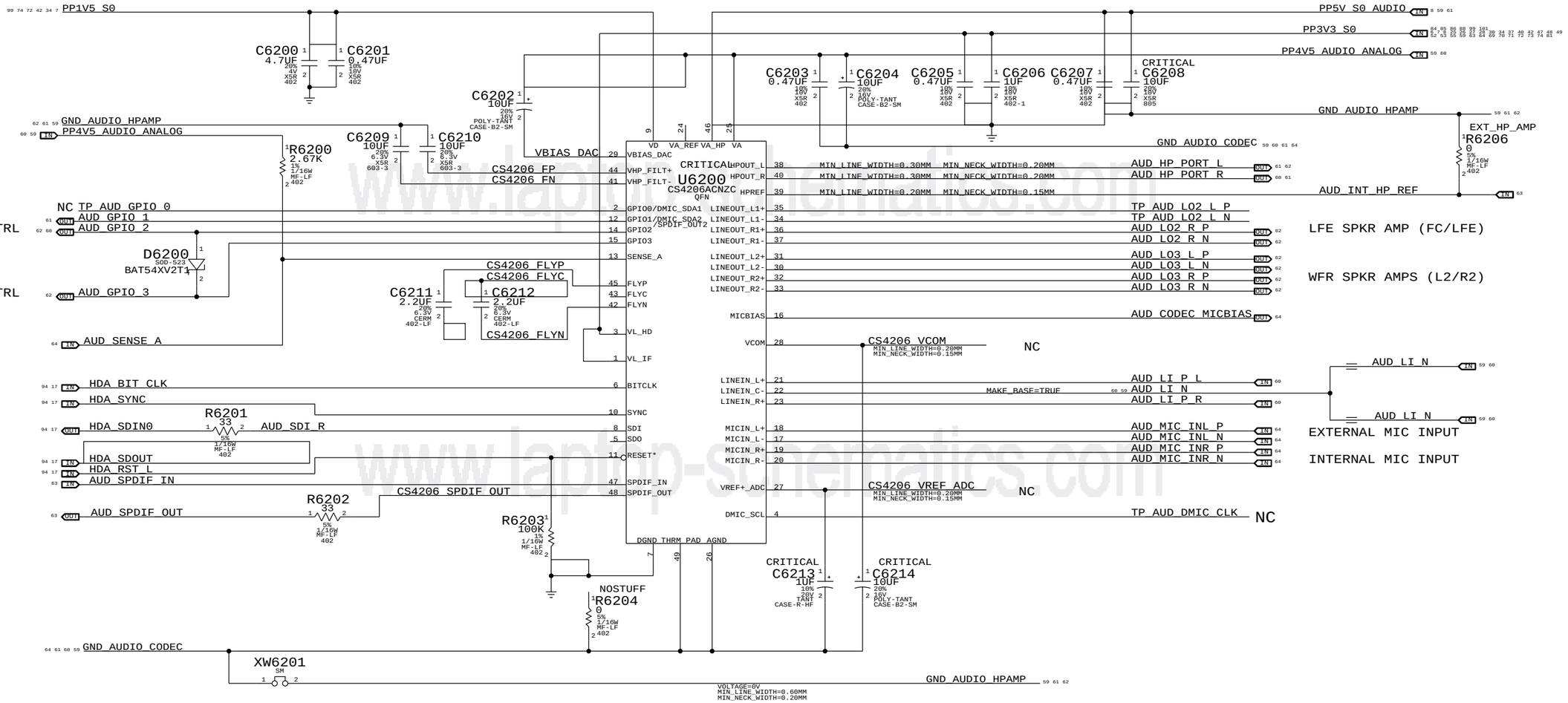
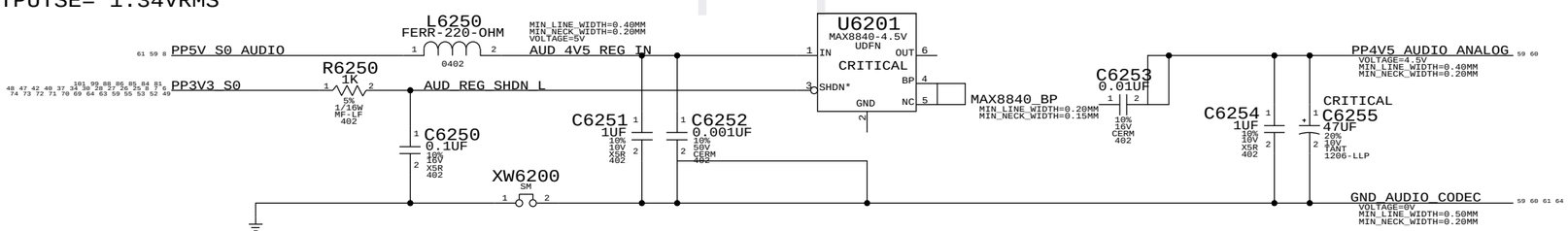
AUDIO CODEC
APPLE P/N 353S2592



DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234



SYNC_MASTER=K17_REF	SYNC_DATE=05/30/2009
PAGE TITLE	AUDIO:CODEC
Apple Inc.	DRAWING NUMBER: SIZE: D
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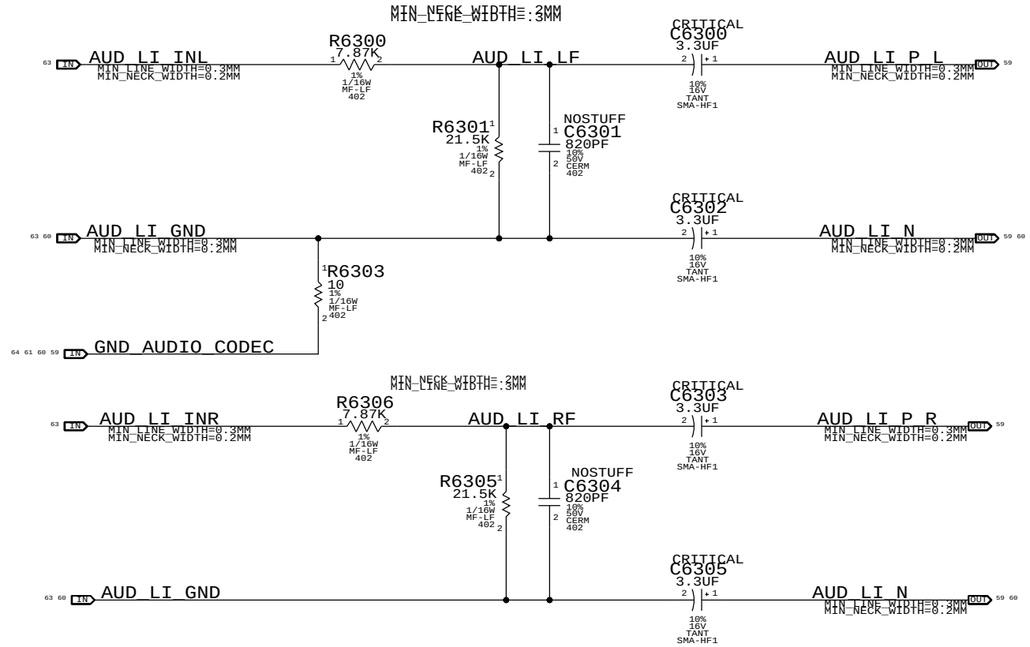
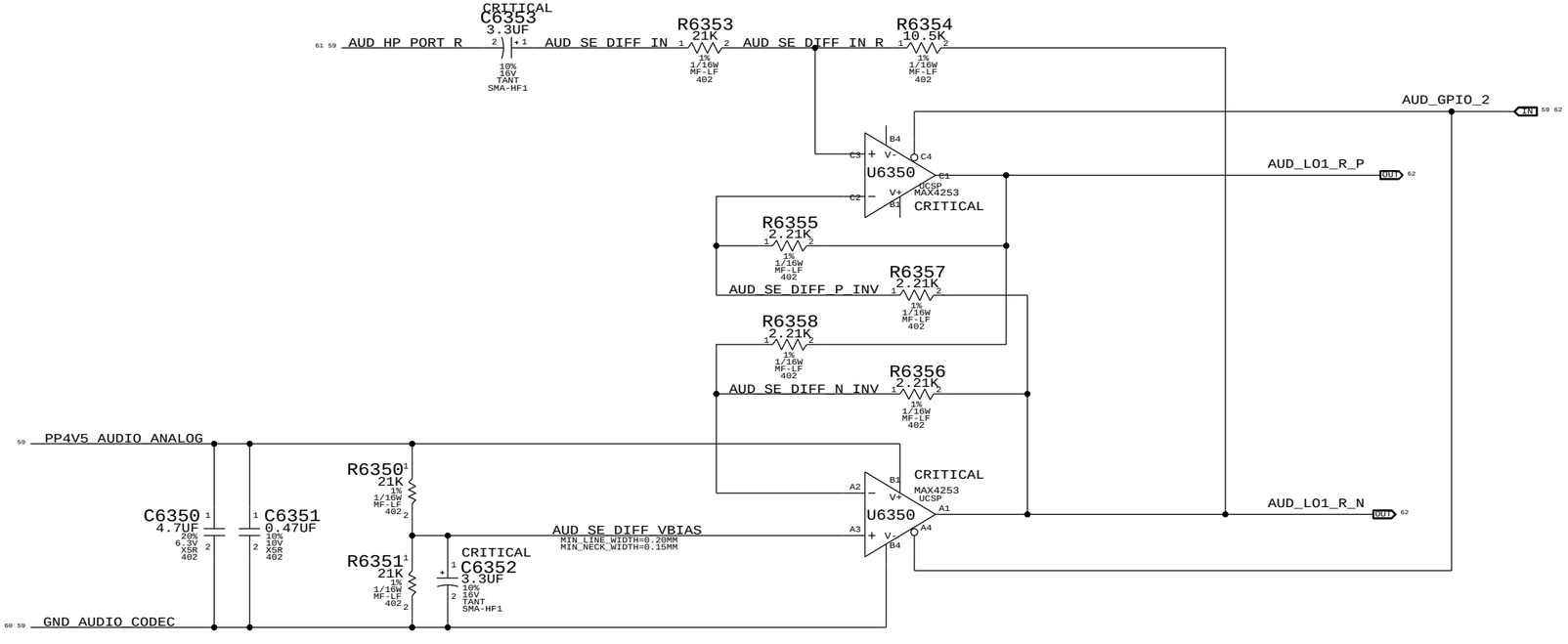
CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SE-TO-DIFF CONVERTER



SYNC_MASTER=K17_REF SYNC_DATE=05/30/2009

PAGE TITLE
AUDIO: LINE IN

Apple Inc.

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HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53

PLACE XW5802 & XW5803 NEAR PP5V_S0_AUDIO

RUN PP5V_AUDIO_HPAMP_* NETS OVER GND

XW6502 SM
PP5V_S0_AUDIO → PP5V_AUDIO_HPAMP_PVDD_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP C6500 10UF 20% 10V X5R 805
EXT_HP_AMP C6501 0.001UF 10% 50V CERM 402

XW6503 SM
PP5V_S0_AUDIO → PP5V_AUDIO_HPAMP_AVDD_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP C6502 10UF 20% 10V X5R 805
EXT_HP_AMP C6503 0.1UF 10% 16V X5R 402

U6500
AK4201EU
USON

AUD_HPAMP_INL_M → LIN
AUD_HPAMP_INR_M → RIN
AUD_GPIO_1 → PDN*
EXT_HP_AMP R6501 0 5% 1/10W MF-LF 402 → AUD_HPAMP_MUTE_L

EXT_HP_AMP R6500 100K 5% 1/10W MF-LF 402

LOUT → AUD_HPAMP_OUTL
ROUT → AUD_HPAMP_OUTR

AK4201 CN
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP CRITICAL C6505 1UF 10% 10V X5R 402

AK4201 CP
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

AK4201 PVEE
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP CRITICAL C6504 1UF 10% 10V X5R 402

AVDD, PVDD, VSS1, VSS2, THRM PAD

AUD_HPAMP_OUTL
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP R6515 0 5% 1/10W MF-LF 603
AUD_HPAMP_OUTL_R
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

AUD_HPAMP_OUTR
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP R6525 0 5% 1/10W MF-LF 603
AUD_HPAMP_OUTR_R
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

R6516 21K 1% 1/10W MF-LF 402
R6526 21K 1% 1/10W MF-LF 402

PLACE XW5800 NEAR U5800 PINS 1/12

XW6500 SM
GND_AUDIO_CODEC → GND_AUDIO_HPAMP_PGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM

EXT_HP_AMP L6535 FERR-220-OHM-2.5A 0603
AUD_LO_GND_R
VOLTAGE=0V
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM

EXT_HP_AMP R6531 13.7K 1% 1/16W MF-LF 402

EXT_HP_AMP R6530 21K 1% 1/10W MF-LF 402
XW6501 SM
AUD_LO_FDBK → AUD_LO_GND_R

AK4201_VSS2
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM

CS4206A HP OUT ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

AUD_HP_PORT_L
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

INT_HP_AMP R6552 0 5% 1/10W MF-LF 603
AUD_HPAMP_OUTL_R

R6550 39 5% 1/10W MF-LF 402
NOSTUFF CRITICAL C6552 2200PF 5% 50V C0G-CERM 603

NC ← AUD_Z_L
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

C6550 0.1UF 10% 16V X7R-CERM 402

INT_HP_AMP R6554 0 5% 1/10W MF-LF 603
AUD_LO_GND_R

GND_AUDIO_HPAMP

C6551 0.1UF 10% 16V X7R-CERM 402

NOSTUFF CRITICAL C6553 2200PF 5% 50V C0G-CERM 603

NC ← AUD_Z_R
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

R6551 39 5% 1/10W MF-LF 402

INT_HP_AMP R6553 0 5% 1/10W MF-LF 603
AUD_HP_PORT_R
AUD_HPAMP_OUTR_R

1ST ORDER DAC FILTER
LP:42.10 KHZ

AUD_HP_PORT_L

EXT_HP_AMP R6510 13.7K 1% 1/16W MF-LF 402
EXT_HP_AMP R6511 21K 1% 1/16W MF-LF 402
AUD_HPAMP_OUTL

NOSTUFF CRITICAL C6511 180PF 5% 50V CERM 402
AUD_HPAMP_INL_M

NOSTUFF CRITICAL C6521 180PF 5% 50V CERM 402
AUD_HPAMP_INR_M

EXT_HP_AMP R6520 13.7K 1% 1/16W MF-LF 402
EXT_HP_AMP R6521 21K 1% 1/16W MF-LF 402
AUD_HP_PORT_R
AUD_HPAMP_OUTR

SYNC_MASTER=K17_REF SYNC_DATE=05/30/2009

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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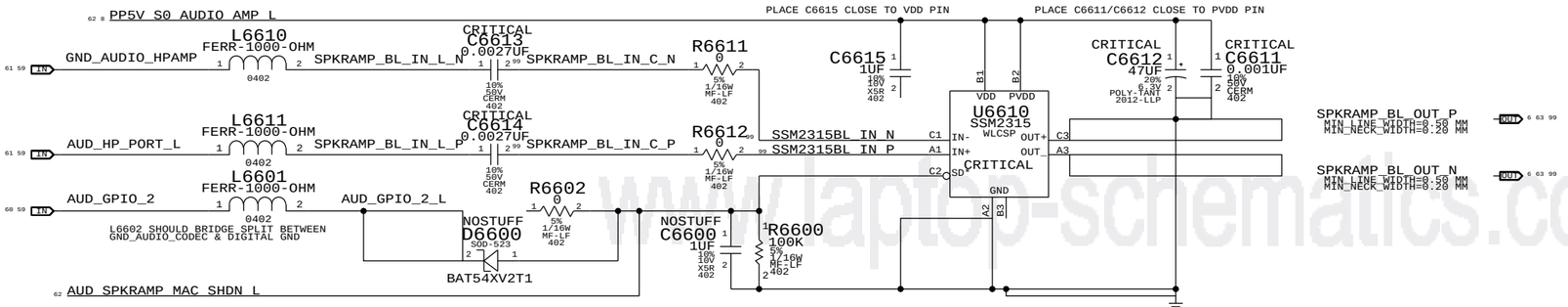
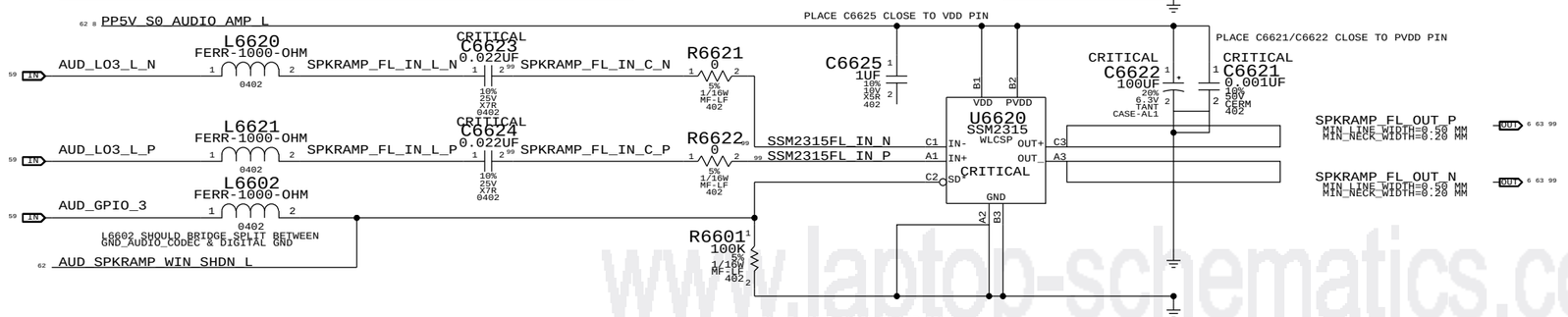
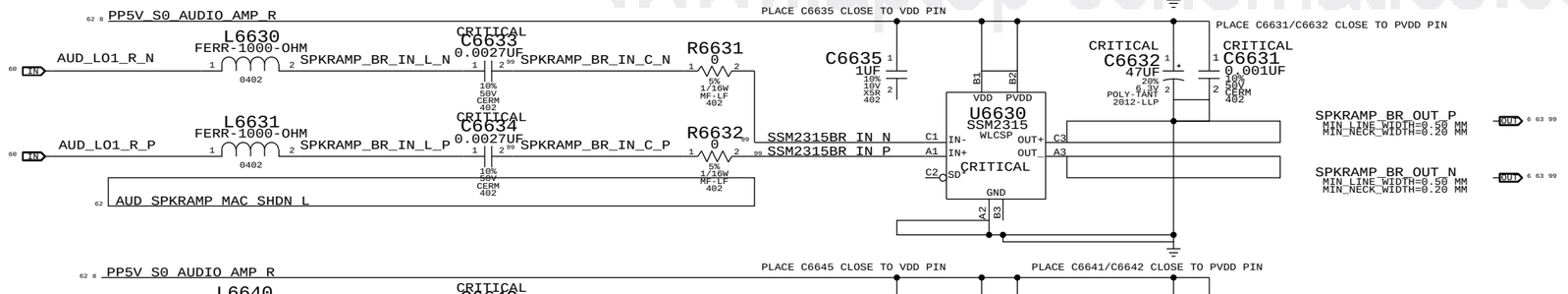
5X MONO SPEAKER AMPLIFIERS (SSM2315)

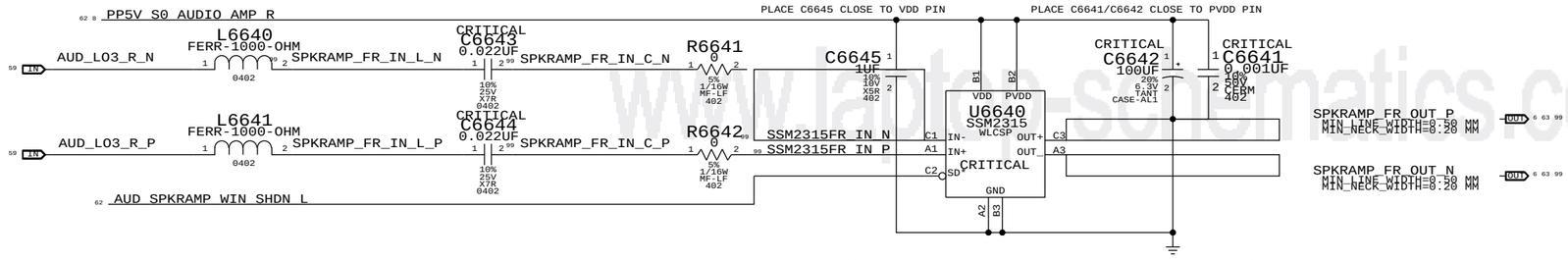
APN: 353S2500
GAIN = +6 DB

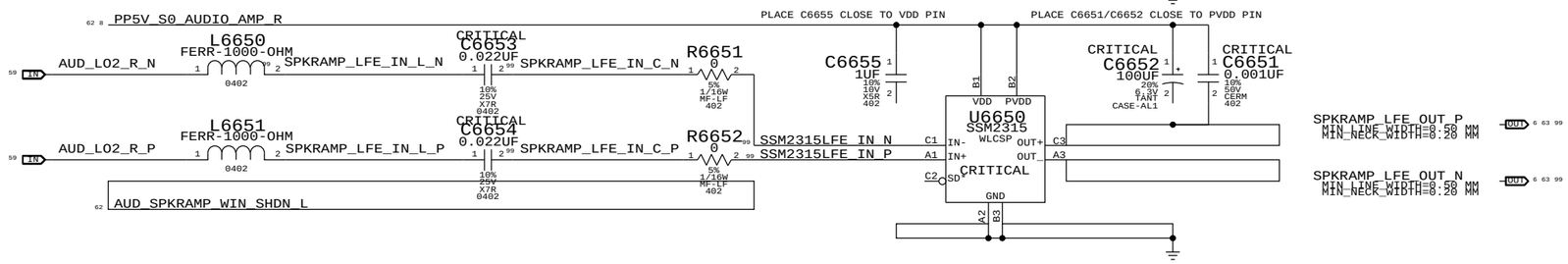
FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ











SYNC MASTER=K17 REF | SYNC DATE=05/30/2009

PAGE TITLE: AUDIO:SPEAKER AMP

Apple Inc.

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AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0

APN: 514-0632

CRITICAL
J6700
SPDIF-TX-K20
F-RT-TH

MICROPHONE 6
DETECT FOR PT 5
SWITCH 2
LEFT 1
RIGHT 3
GROUND 4

AUDIO
A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10 11 12 13
SHIELD PINS

C6700 1UF 10% 10V X5R 402

AUD_CONNJ1_SLEEVE2 (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ1_SLEEVEDET (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ1_TIPDET (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ1_TIP (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ1_RING (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ1_SLEEVE (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)

L6700 FERR-1000-OHM 0402 → HS_MIC_HI (OUT 64)
R6701 10K 5% 1/16W MF-LF 402
L6702 FERR-1000-OHM 0402 → AUD_J1_SLEEVEDET_R (OUT 64)
L6703 FERR-1000-OHM 0402 → AUD_J1_PERIPHDET_R (OUT 64)
L6704 CRITICAL FERR-220-OHM 0402 → AUD_J1_TIPDET_R (OUT 64)
L6705 CRITICAL FERR-220-OHM 0402 → AUD_HPAMP_OUTL_R (BI 61)
L6706 FERR-1000-OHM 0402 → AUD_HPAMP_OUTR_R (BI 61)
L6707 CRITICAL FERR-220-OHM-2.5A 0603 → HS_MIC_LO (OUT 64)
AUD_LO_GND_R (OUT 61)
AUD_SPDIF_OUT (IN 59)

CRITICAL DZ6700 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402

GND_CHASSIS_AUDIO_JACK (MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.10MM, VOLTAGE=0V) 63

MIC CONNECTOR
APN: 518S0520

L6781 FERR-1000-OHM 0402
INT_MIC_F_N (OUT 64) → INT_MIC_N
INT_MIC_SHIELD (6) → INT_MIC_P
L6780 FERR-1000-OHM 0402
INT_MIC_F_P (OUT 64)
R6780 0 5% 1/16W MF-LF 402

CRITICAL J6780 78171-0003 M-RT-SM

SPEAKER CONNECTORS
APN: 518S0521

INT_HP_AMP
R6709 0 5% 1/16W MF-LF 402
AUD_INT_HP_REF (59)

SPKRAMP_FL_OUT_P (IN 62)
SPKRAMP_FL_OUT_N (IN 62)
SPKRAMP_BL_OUT_P (IN 62)
SPKRAMP_BL_OUT_N (IN 62)

NOSTUFF C6781 100PF 5% 50V CERM 402
NOSTUFF C6782 100PF 5% 50V CERM 402
NOSTUFF C6783 100PF 5% 50V CERM 402
NOSTUFF C6784 100PF 5% 50V CERM 402

CRITICAL J6781 78171-0004 M-RT-SM

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0

APN: 514-0633

CRITICAL
J6750
SPDIF-RX-K20
F-RT-TH

DETECT FOR PT 5
SWITCH 2
LEFT 1
RIGHT 3
GROUND 4

AUDIO
A - VDD 6
B - GND 7
C - VOUT 8
OPERATING VOLTAGE 3.3
POF

SHELL 9 10 11 12
SHIELD PINS

C6750 1UF 10% 10V X5R 402

AUD_CONNJ2_TIPDET (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ2_TIP (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ2_RING (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_CONNJ2_SLEEVE (MIN_LINE_WIDTH=0.40MM, MIN_NECK_WIDTH=0.20MM)
AUD_J2_OPT_OUT

L6751 FERR-1000-OHM 0402 → AUD_J2_TIPDET_R (OUT 64)
L6752 FERR-1000-OHM 0402 → AUD_LI_INL (BI 60)
L6753 FERR-1000-OHM 0402 → AUD_LI_INR (BI 60)
L6754 600-OHM-300MA 0402 → AUD_LI_GND (OUT 60)
R6755 10 5% 1/16W MF-LF 402 → AUD_SPDIF_IN (OUT 59)

CRITICAL DZ6753 ESDALC5-1BM2 SOD882
CRITICAL DZ6750 ESDALC5-1BM2 SOD882
CRITICAL DZ6751 6.8V-100PF 402
CRITICAL DZ6752 6.8V-100PF 402

GND_CHASSIS_AUDIO_JACK (63)

RETURN FOR HF NOISE
R6750 0 5% 1/16W MF-LF 402

APN: 518S0672

CRITICAL J6782 78171-6006 M-RT-SM

SPKRAMP_FR_OUT_P (IN 62)
SPKRAMP_FR_OUT_N (IN 62)
SPKRAMP_BR_OUT_P (IN 62)
SPKRAMP_BR_OUT_N (IN 62)
SPKRAMP_LFE_OUT_P (IN 62)
SPKRAMP_LFE_OUT_N (IN 62)

NOSTUFF C6785 100PF 5% 50V CERM 402
NOSTUFF C6786 100PF 5% 50V CERM 402
NOSTUFF C6787 100PF 5% 50V CERM 402
NOSTUFF C6788 100PF 5% 50V CERM 402
NOSTUFF C6789 100PF 5% 50V CERM 402
NOSTUFF C6790 100PF 5% 50V CERM 402

SYNC_MASTER=K17_LENGO SYNC_DATE=11/24/2009

PAGE TITLE: AUDIO: JACKS

Apple Inc.

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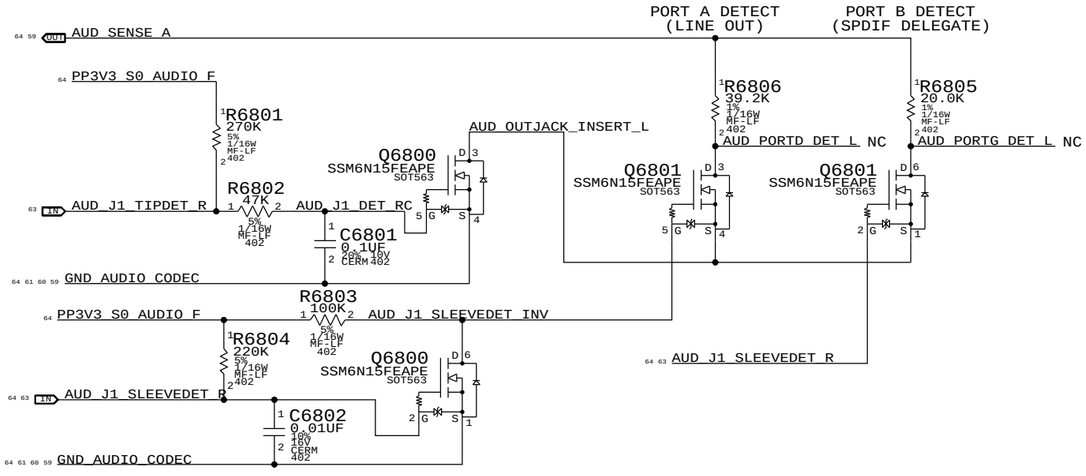
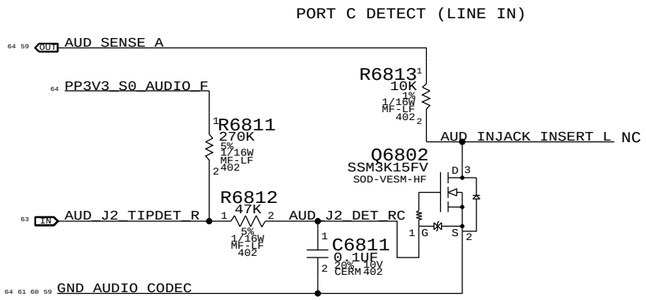
CODEC OUTPUT SIGNAL PATHS

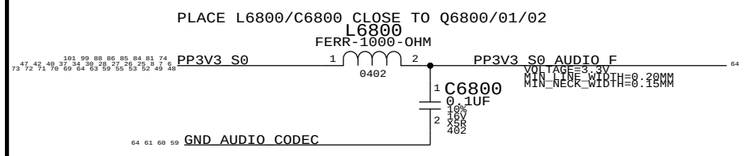
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

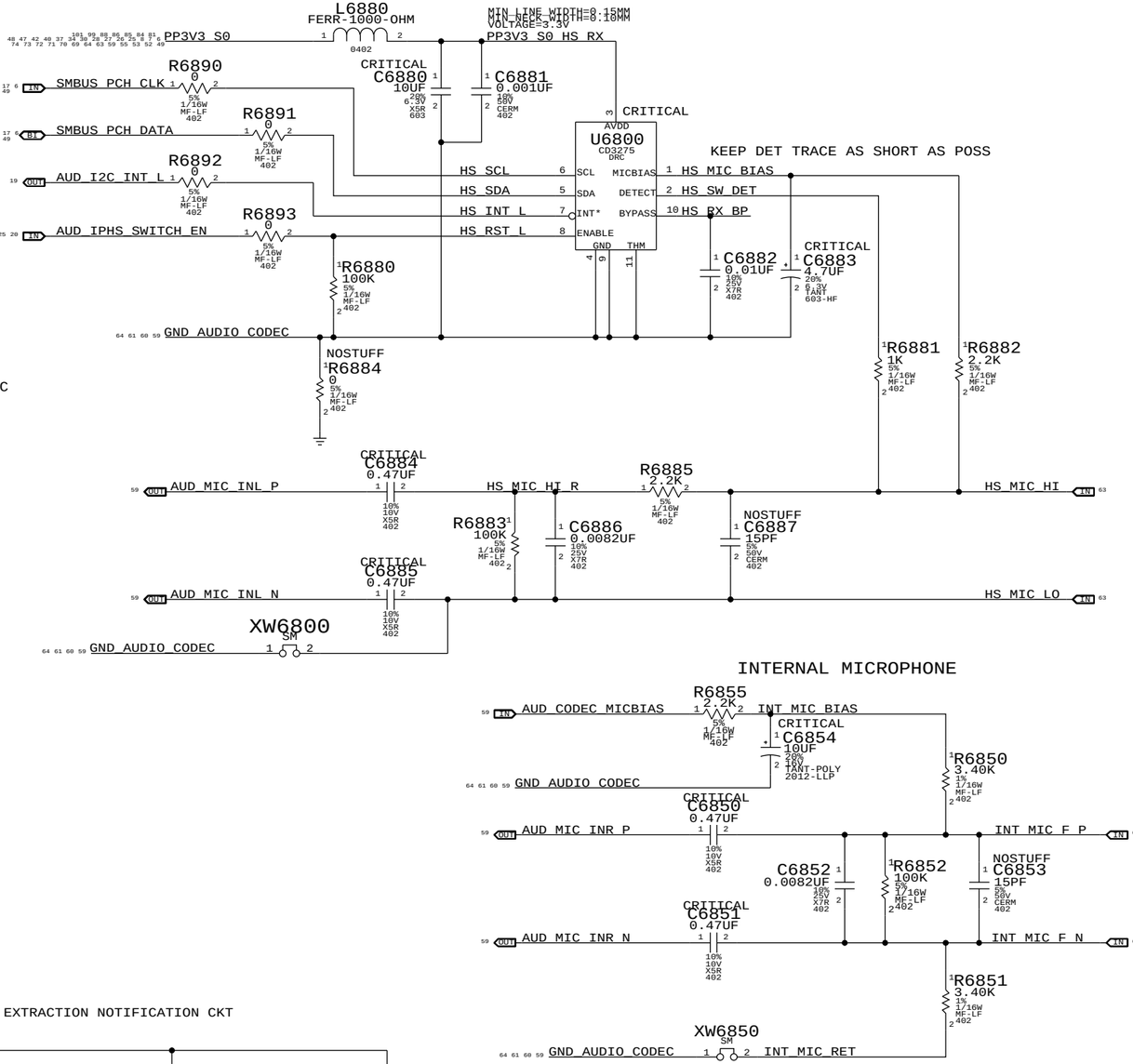
CODEC INPUT SIGNAL PATHS

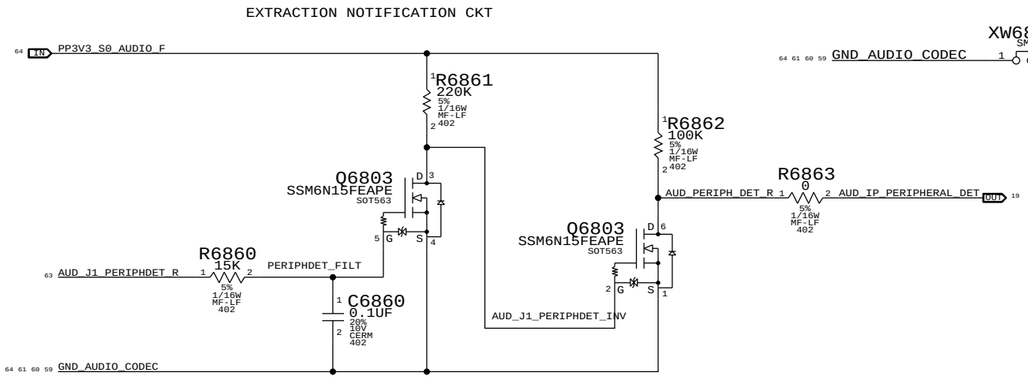
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY











SYNC MASTER=K17 REF SYNC DATE=05/30/2009

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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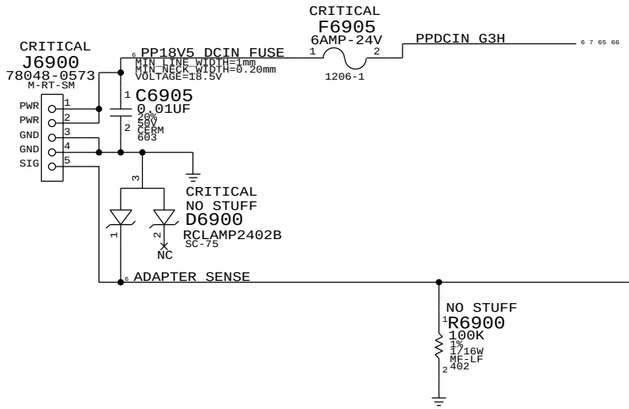
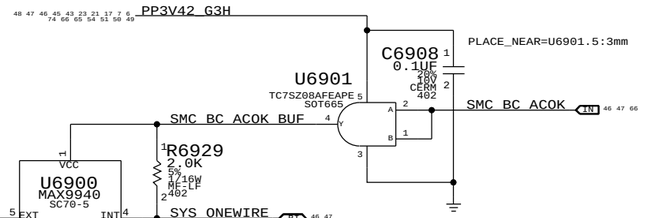
MagSafe DC Power Jack

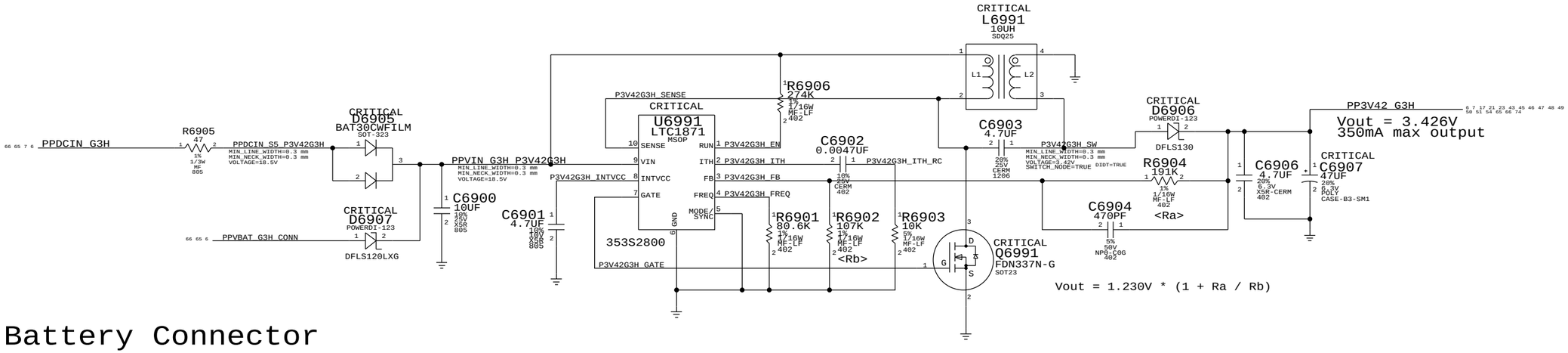


1-Wire OverVoltage & ESD Protection

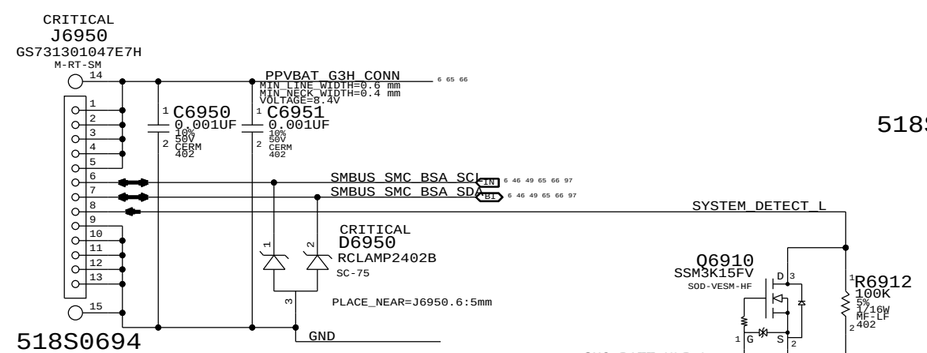


3.425V "G3Hot" Supply

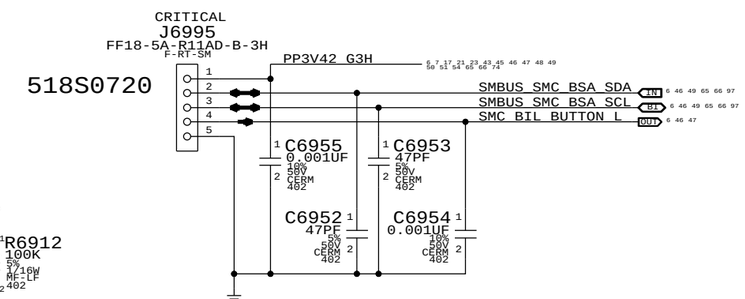
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Battery Connector



BIL Connector



SYNC_MASTER=K17_REF SYNC_DATE=04/29/2009

PAGE TITLE
DC-In & Battery Connectors

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Reverse-Current Protection

Inrush Limiter

FROM ADAPTER
PPDCIN_G3H

CRITICAL Q7080 HAT1128R01 SOI

CRITICAL Q7085 HAT1128R01 SOI

PPDCIN_G3H_OR_PBUS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

R7080 100K 5% 1/16W MF-LF 402
C7085 0.1UF 10% 25V X5R 402
R7085 470K 1% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm
R7081 62K 5% 1/16W MF-LF 402

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm
R7086 332K 1% 1/16W MF-LF 402

CRITICAL D7005 BAT30CWFILM SOT-323

R7003 20 5% 1/16W MF-LF 402 CHGR_DCIN_R

(CHGR_SGATE)
(CHGR_DCIN)
(CHGR_AGATE)

ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 16V X5R 402

PP3V42_G3H

R7010 30.1K 1% 1/16W MF-LF 402

NO STUFF R7002 100K 5% 1/16W MF-LF 402

R7000 0 5% 1/16W MF-LF 402

SMC_RESET_L

U7000 ISL6259HRTZ TQFN

VDD	19		
VDDP	20		
VHST	12	CRITICAL DCIN	2 CHGR_DCIN
SMB_RST_N	13	SGATE	26 CHGR_SGATE
SCL	11	AGATE	1 CHGR_AGATE
SDA	10	CSIP	28 CHGR_CSI_P
VFRQ	4	CSIN	27 CHGR_CSI_N
CELL	6	BOOT	25 CHGR_BOOT
ACIN	3	UGATE	24 CHGR_UGATE
ICOMP	5	PHASE	23 CHGR_PHASE
VCOMP	7	LGATE	21 CHGR_LGATE
VNEG	8	BGATE	16 CHGR_BGATE
CSOP	18	20V/V AMON	9 CHGR_AMON
CSON	17	36V/V BMON	15 CHGR_BMON
(AGND) THRM_PAD	29	(OD) ACOK	14 SMC_BC_ACOK
PGND	22		

SMC_RESET_L
SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
CHGR_RST_L

Float CELL for 1S

R7011 9.31K 1% 1/16W MF-LF 402
R7013 100 1% 1/16W MF-LF 402
R7015 220K 5% 1/16W MF-LF 402
R7016 3.01K 1% 1/16W MF-LF 402

C7050 1UF 10% 16V X5R 402
C7015 470PF 10% 25V CERM 402
C7016 470PF 10% 25V CERM 402

CHGR_VCOMP_R
CHGR_VNEG_R

C7042 0.068UF 10% 10V CERM 402
C7002 1UF 10% 10V X5R 402
C7011 0.01UF 10% 16V CERM 402
C7000 1UF 10% 10V X5R 402-1
C7005 0.22UF 20% 25V CERM 805
C7026 0.001UF 10% 50V CERM 402

XW7000 SM
PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

353S2392

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

(GND)
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)

R7051 2.2 5% 1/16W MF-LF 402 CHGR_CSO_R_P
R7052 0 5% 1/16W MF-LF 402 CHGR_CSO_R_N

R7021 10 5% 1/16W MF-LF 402
R7022 10 5% 1/16W MF-LF 402

CHGR_CSI_R_P
CHGR_CSI_R_N

C7020 0.047UF 10% 10V CERM 402
C7022 0.1UF 10% 25V X5R 402
C7021 0.1UF 10% 25V X5R 402
C7025 0.22UF 10% 10V CERM 402

CRITICAL R7020 0.020 0.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL Q7031 RJK0305DPB LFPAK-HF

CRITICAL Q7030 RJK0305DPB LFPAK-HF

Max Current = 15A
(L7030/L7031 limit)
f = 400 kHz

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM
CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM
CRITICAL C7032 22UF 20% 25V POLY-TANT CASE-D2-SM
CRITICAL C7033 22UF 20% 25V POLY-TANT CASE-D2-SM
C7035 1UF 10% 25V X5R 603-1
C7036 1UF 10% 25V X5R 603-1
C7037 0.001UF 10% 50V X7R 402

CRITICAL L7030 2.2UH-20A-5.5M-OHM SM
CRITICAL L7031 2.2UH-20A-5.5M-OHM SM

CHGR_PHASE_MID
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

CRITICAL F7040 8AMP-24V 1206
CRITICAL F7041 8AMP-24V 1206

TO SYSTEM
PPBUS_G3H

NO STUFF R7039 10 5% 1/10W MF-LF 603
CHGR_PHASE_RC

NO STUFF C7039 0.001UF 10% 50V X7R 402

CRITICAL Q7035 RJK0305DPB LFPAK-HF

CRITICAL Q7036 RJK0305DPB LFPAK-HF

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

CRITICAL C7040 33UF 20% 16V POLY-TANT CASED2E-SM
CRITICAL C7041 33UF 20% 16V POLY-TANT CASED2E-SM
C7045 0.001UF 10% 50V X7R 402

CRITICAL R7050 0.005 1% 1W MF 0612

TO/FROM BATTERY
PPVBAT_G3H_CONN

CRITICAL Q7055 SI7137DP SO-8
CRITICAL Q7056 SI7137DP SO-8

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

PPVBAT_G3H_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

C7055 1UF 10% 25V X5R 603-1
C7056 0.1UF 10% 16V X5R 402
C7057 0.01UF 10% 16V CERM 402

C7058 1UF 10% 16V X5R 402
R7058 1M 1% 1/10W MF-LF 402
R7059 20K 5% 1/10W MF-LF 402

BATT_POS_GATE
GND

R7092 1K 5% 1/10W MF-LF 402 CHGR_BGATE_R

R7093 220K 5% 1/16W MF-LF 402 CHGR_OVP_G_C

PLACE_NEAR=Q7055.4:1mm

CRITICAL U7090 SOT-363 ASMCC0178

CHGR_OVP_A
CHGR_OVP_B

R7094 1K 5% 1/16W MF-LF 402

C7090 100PF 5% 50V CERM 402
R7090 20K 5% 1/16W MF-LF 402

PLACE_NEAR=U7090.5:1mm

SYNC_MASTER=K17_REF
SYNC_DATE=04/29/2009

PAGE TITLE
PBus Supply & Battery Charger

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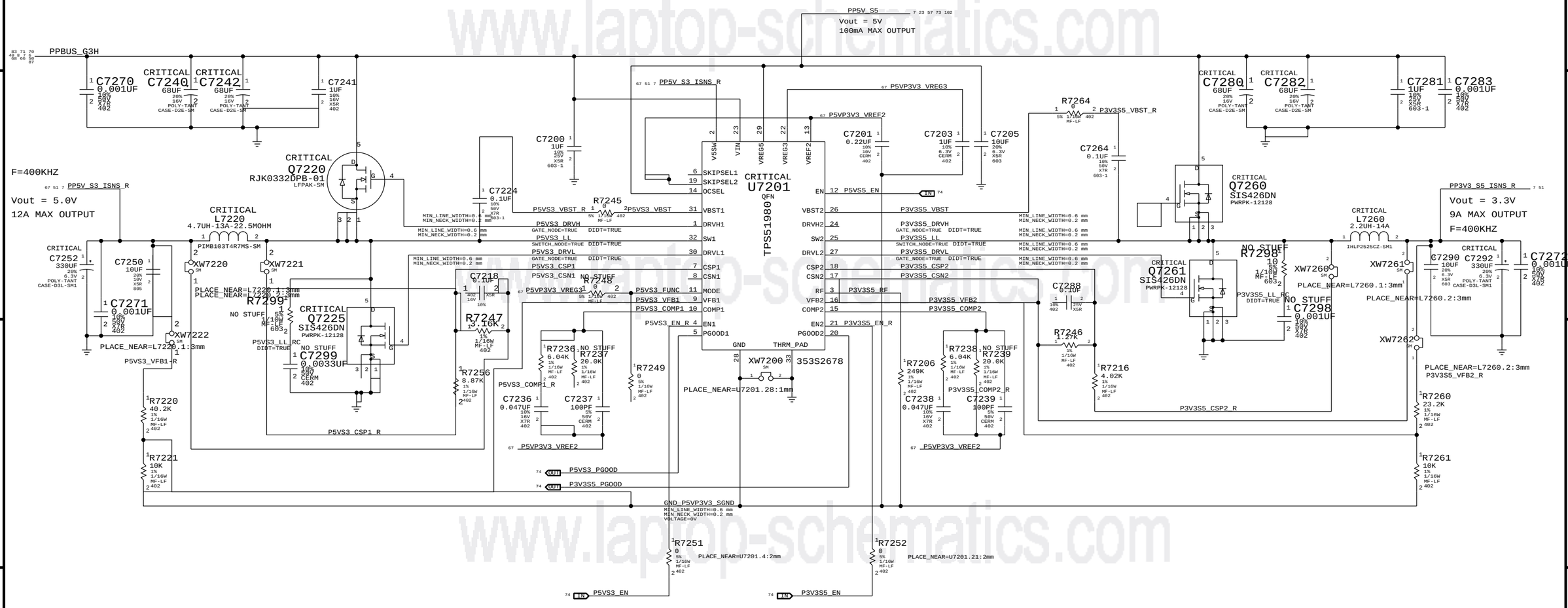

SYNC_MASTER=K20A_MLB	SYNC_DATE=03/26/2009
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER: SIZE D
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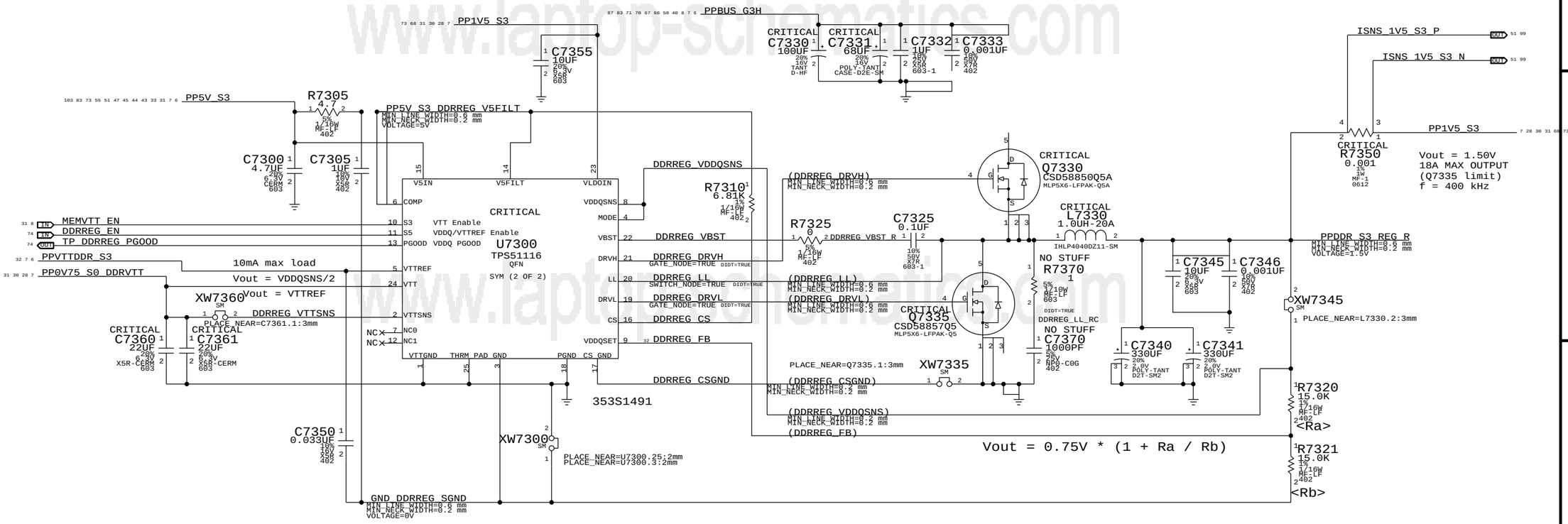

SYNC_MASTER=K17_REF SYNC_DATE=06/24/2009

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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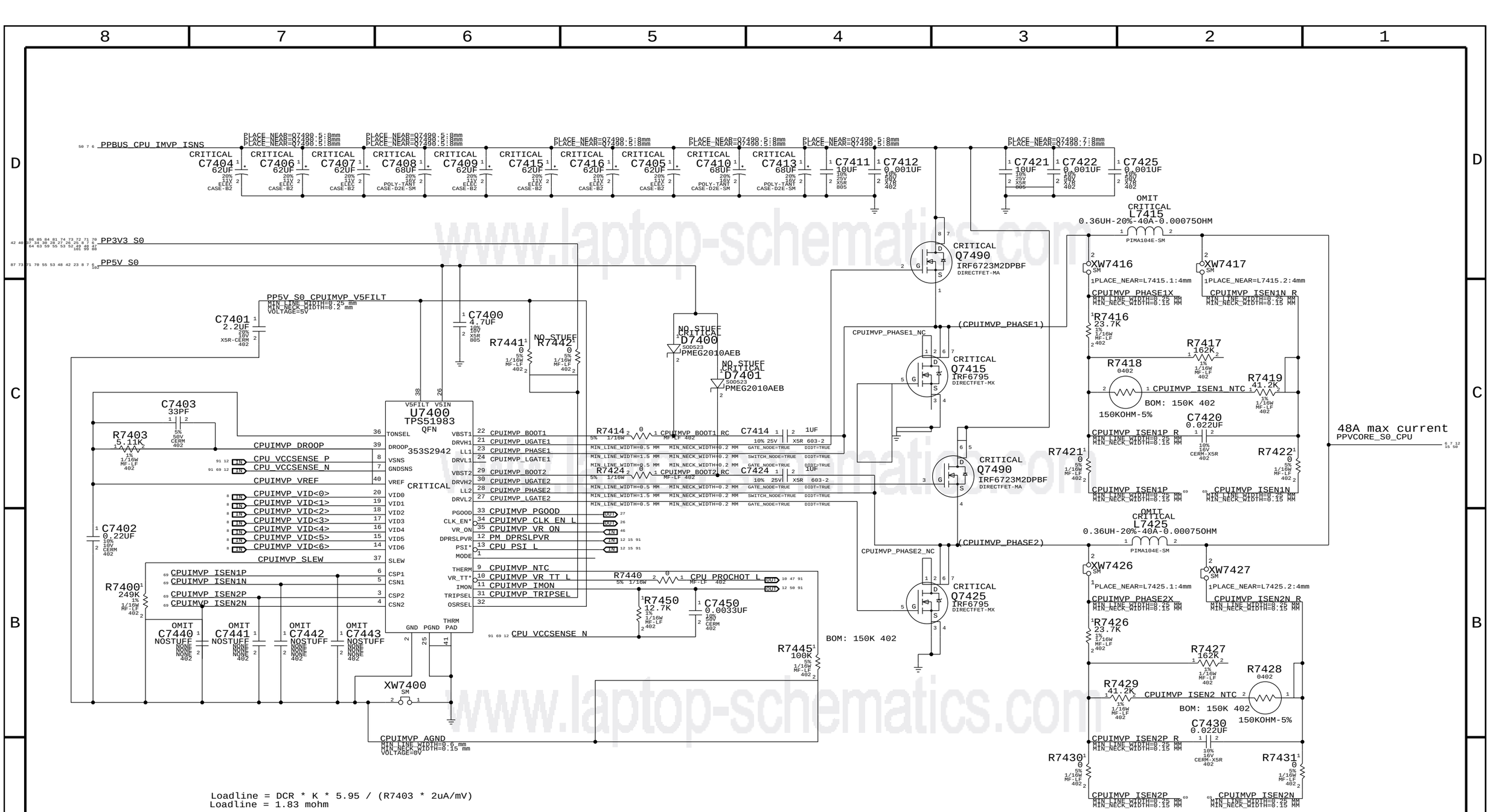

Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

VIMON = Io * DCR * K * 2uA/mV * R7450
50 A = 1.049 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.787

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1177	2	IND,PWR,0.36uH,1.05MO,12x10x4mm	L7415,L7425	CRITICAL	

SYNC_MASTER=K18_POWER SYNC_DATE=06/29/2009

PAGE TITLE: CPU IMVP VCore Regulator

Apple Inc.

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PPBUS_G3H
PP5V_S0
PP3V3_S0
GFXIMVP_DROOP
R7512 1K 1/10W MF-LF 402
C7511 33PF 5% 50V C0GM 402
R7511 1.69K 1% 1/16W MF-LF 402
C7510 2.2UF 10% 16V X5R 603
C7513 2.2UF 10% 16V X5R 603
R7514 0 5% 1/10W MF-LF 402
D7514 BAT30CWFILM SOT-323
GFXIMVP_VBST_R
GFXIMVP_UGATE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE
C7524 0.001UF 10% 50V X7R CERM 402
C7520 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7521 100UF 20% 16V TANT D-HF
C7523 1UF 10% 25V X5R 0603-1
CRITICAL
Q7530 CSD58850Q5A MLP5X6-LFPAK-Q5A
GFXIMVP_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE
L7530 0.47UH-26A IHLP2525CZERR47M01
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V
R7540 0.001 1% 1W MF-1 0612
PPVCORE_S0_GFX_REG_R
PPVCORE_S0_GFX
Vout = VID controlled
22A max output
f = 350KHz
NO STUFF
R7570 1 5% 1/10W MF-LF 603
Q7535 CSD58857Q5 MLP5X6-LFPAK-Q5
GFXIMVP_LL_RC
NO STUFF
C7570 1000PF 5% 25V NP0-C0G 402
C7556 10UF 20% 6.3V X5R 603
C7557 0.001UF 10% 50V CERM 402
U7500 TPS51981 QFN
V5IN
DROOP
TONSEL
VSNS
GNDSNS
VREF
VID0
VID1
VID2
VID3
VID4
VID5
VID6
ISLEW
CSP
CSN
V5FILT
VBST
DRVH
LL
DRVL
PGOOD
CLK_EN*
VR_ON
DPRSLPVR
MODE
IMONC
TRIPSEL
IMON
VR_TT*
THERM
PP5V_S0_GFXIMVP_V5FILT
GFXIMVP_VBST
TP_GFXIMVP_PGOOD
GFX_VR_EN
GFX_DPRSLPVR
GFXIMVP_OSRSEL
GFXIMVP_TRIPSEL
GFXIMVP_IMON
GFXIMVP_THERM
GFXIMVP_VREF
GFX_VSENSE_P
GFX_VSENSE_N
GFXIMVP_VID<0>
GFXIMVP_VID<1>
GFXIMVP_VID<2>
GFXIMVP_VID<3>
GFXIMVP_VID<4>
GFXIMVP_VID<5>
GFXIMVP_VID<6>
GFXIMVP_ISLEW
GFXIMVP_CS_P
GFXIMVP_CS_N
GFXIMVP_CS_R_N
GFXIMVP_CS_R_P
R7510 0 5% 1/10W MF-LF 402
R7513 46.4K 1% 1/16W MF-LF 402
R7516 150K 1% 1/16W MF-LF 402
R7517 100K 1% 1/16W MF-LF 402
R7515 22.6K 1% 1/16W MF-LF 402
R7518 200K 1% 1/16W MF-LF 402
R7542 0 5% 1/16W MF-LF 402
R7541 0 5% 1/16W MF-LF 402
C7512 0.22UF 10% 16V CERM 402
C7549 10PF 5% 50V CERM 402
C7542 OMIT NOSTUFF NONE NONE 402
C7541 OMIT NOSTUFF NONE NONE 402
C7515 0.0033UF 10% 16V CERM 402
C7517 0.022UF 10% 16V CERM-X5R 402
XW7500 353S2664 SM
PLACE_NEAR=U7500.1:1mm
PLACE_NEAR=U7500.33:1mm
GND_GFXIMVP_AGND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
(GND_GFXIMVP_AGND)
(GFX_VSENSE_N)
SIGNAL_MODEL=EMPTY
NC

Imon = Io x R7540 x 2uA/mV x R7515
Imon = Io x 45.2 mV/A
22A => 995mV

SYNC_MASTER=T22_MLB SYNC_DATE=03/26/2009

PAGE TITLE
GFX IMVP VCore Regulator

Apple Inc.

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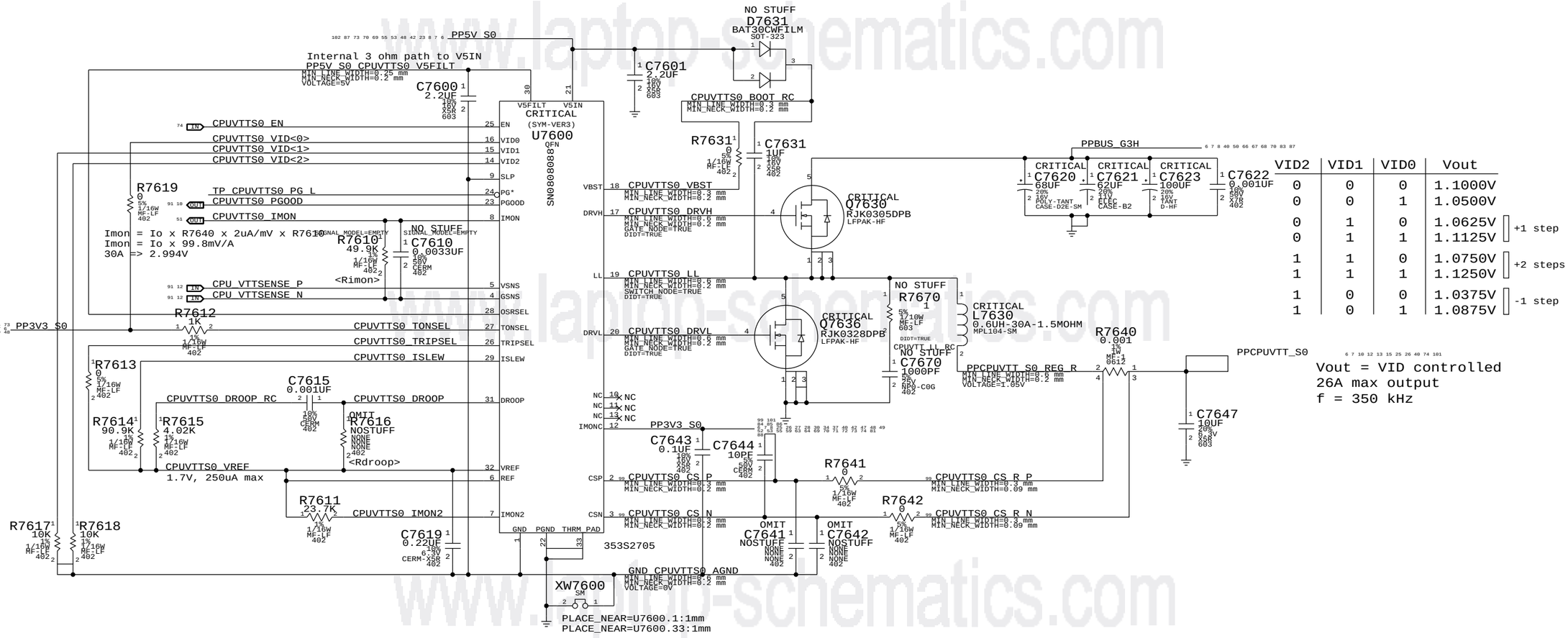
CPU VTT (1.05V S0) Regulator



VID2	VID1	VID0	Vout	
0	0	0	1.1000V	
0	0	1	1.0500V	
0	1	0	1.0625V	+1 step
0	1	1	1.1125V	
1	1	0	1.0750V	+2 steps
1	1	1	1.1250V	
1	0	0	1.0375V	-1 step
1	0	1	1.0875V	

Vout = VID controlled
26A max output
f = 350 kHz

SYNC_MASTER=T22_MLB SYNC_DATE=03/26/2009

PAGE TITLE: CPUVTT (1.05V) Power Supply

Apple Inc.

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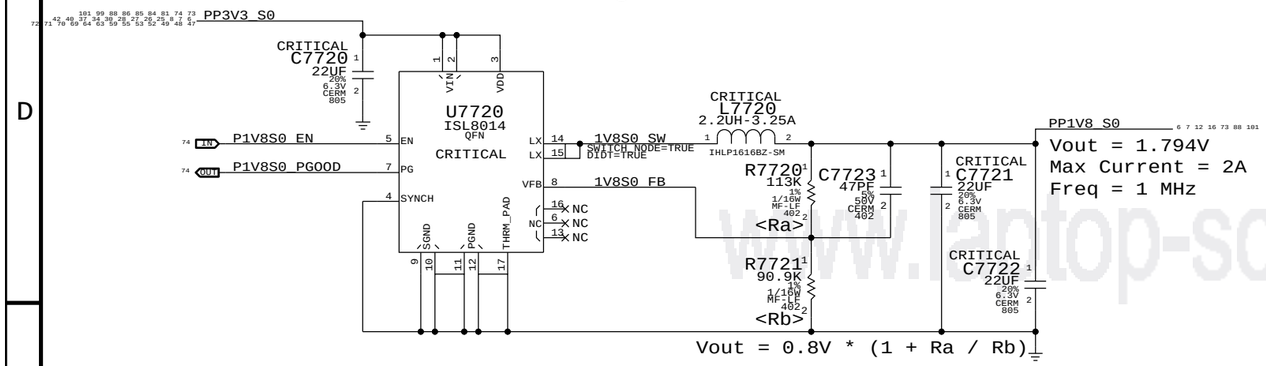
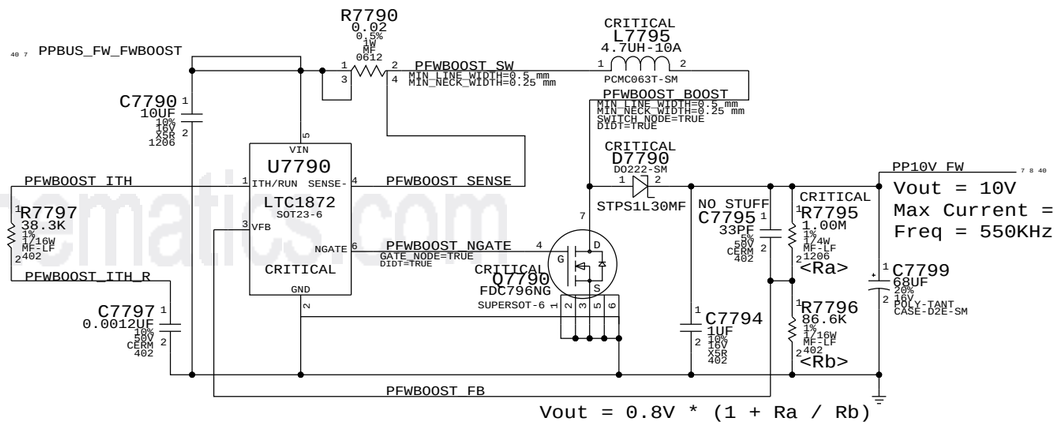
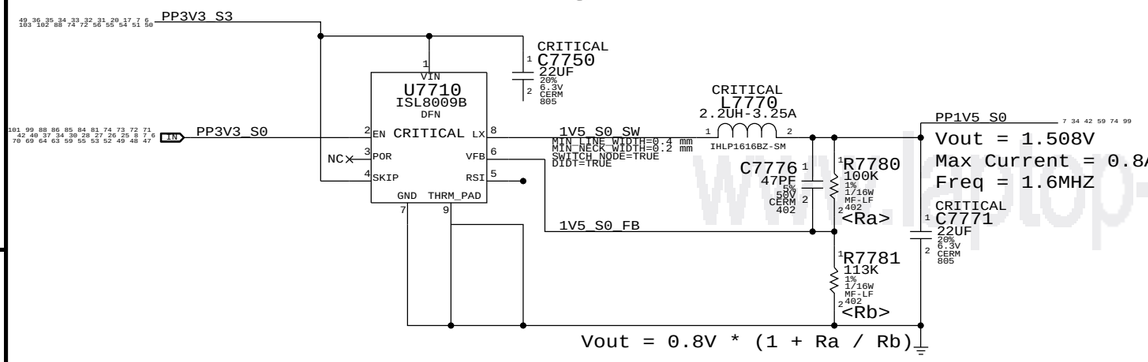
1.8V S0 Regulator



FW 10V Boost Regulator

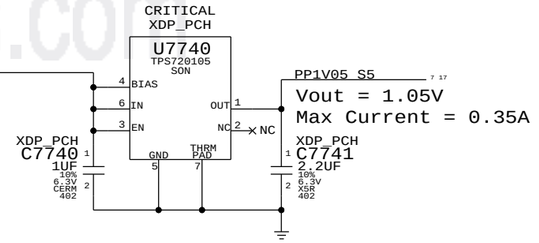


1.5V S0 Regulator

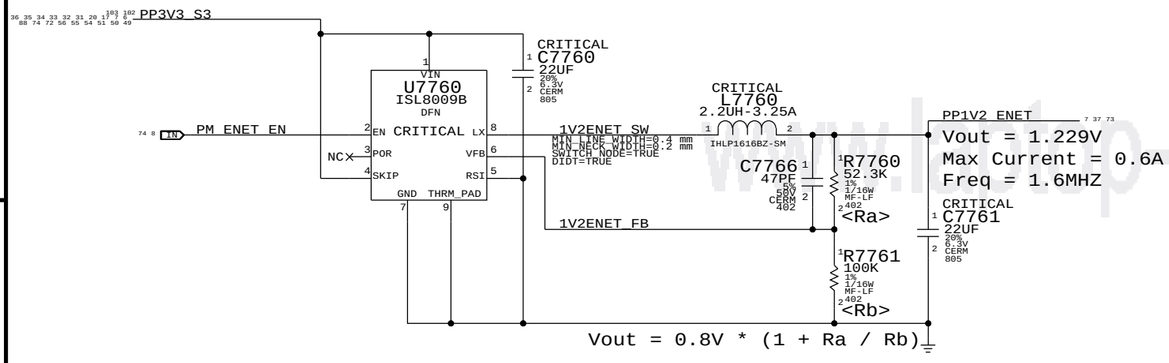


1.05V S5 LDO

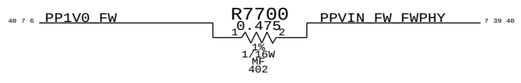
Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.2V ENET Regulator



1.05V to 1.0V FW Drop



SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Misc Power Supplies

Apple Inc.

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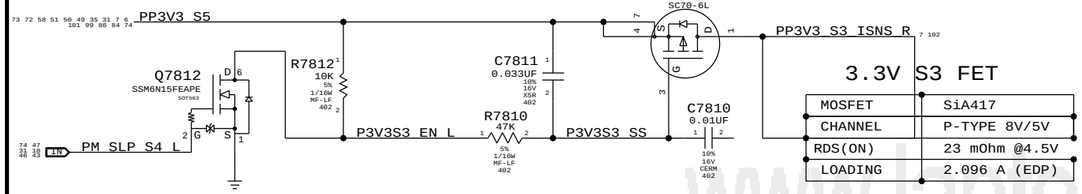
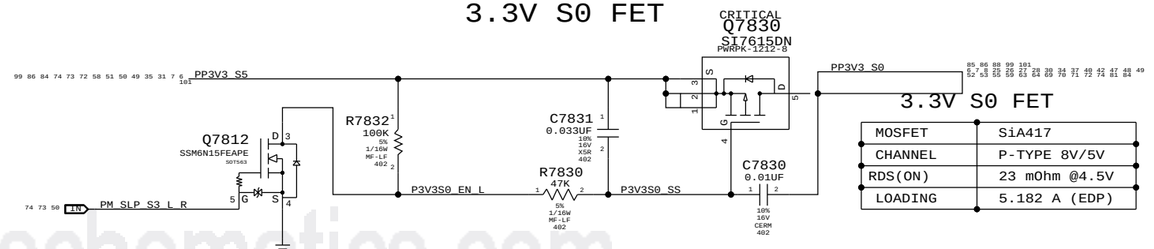
3.3V S3 FET



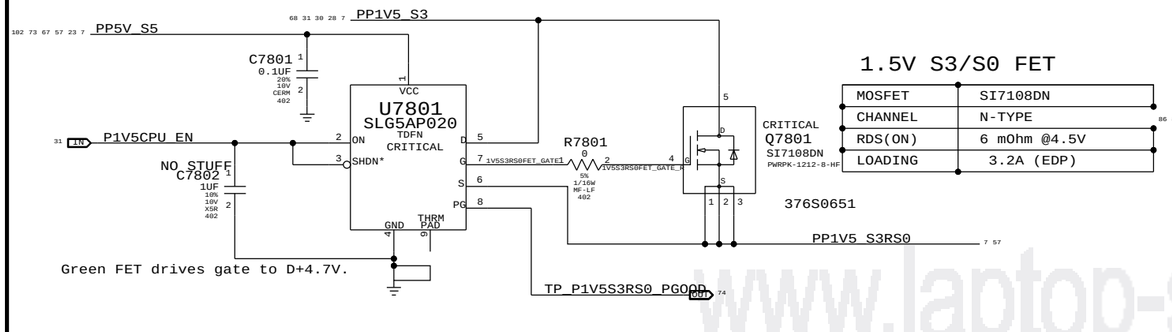
3.3V S3 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.096 A (EDP)

3.3V S0 FET



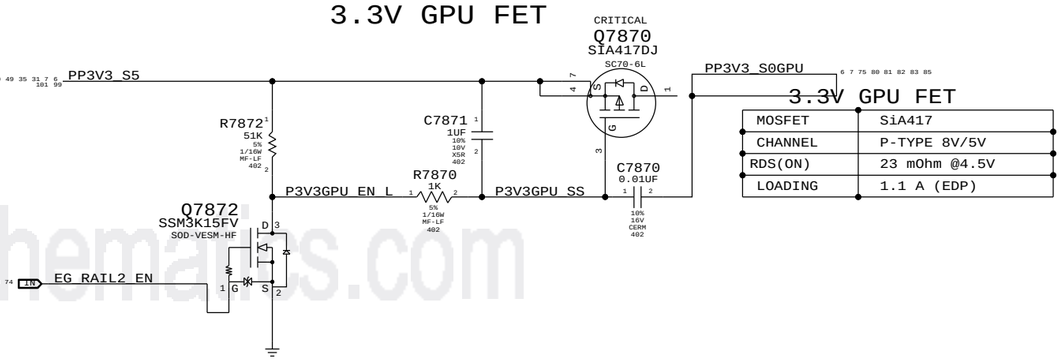
3.3V S0 FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	5.182 A (EDP)

1.5V S3/S0 FET



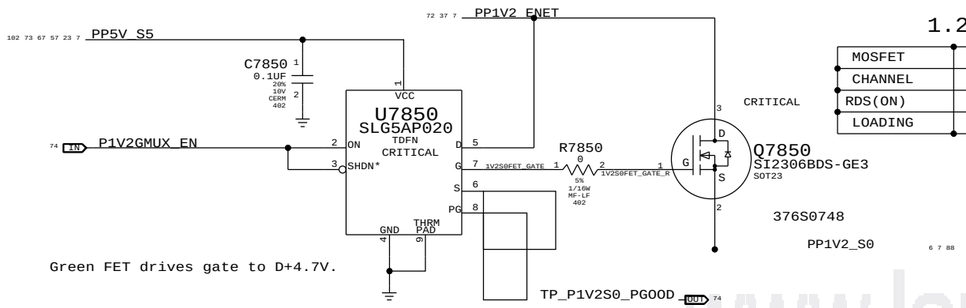
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2A (EDP)

3.3V GPU FET



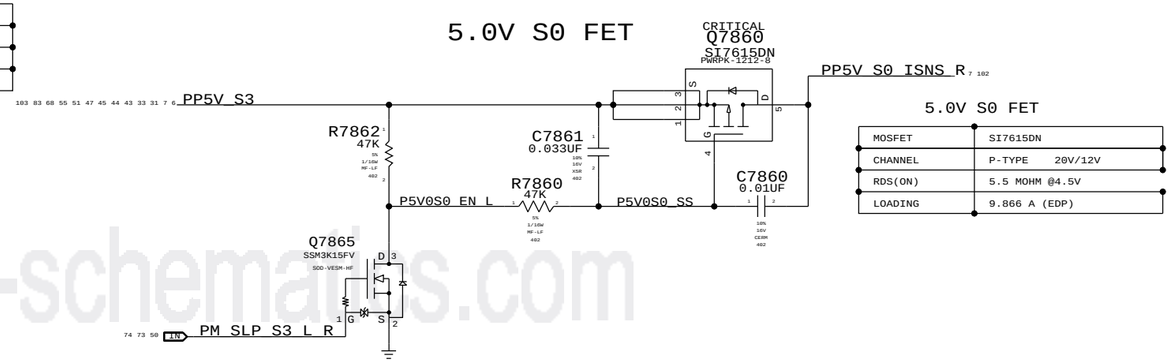
3.3V GPU FET	
MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.1 A (EDP)

1.2V S0 FET



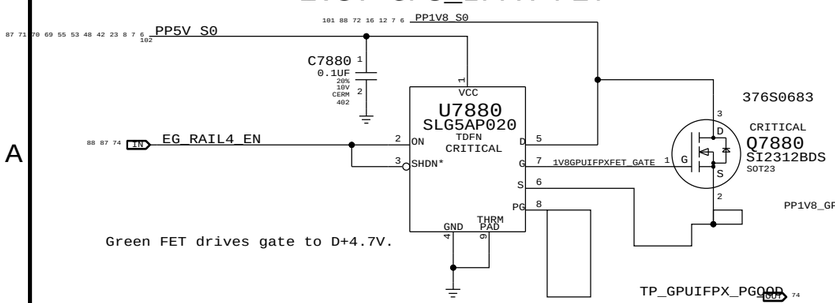
1.2V S0 FET	
MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	9.866 A (EDP)

1.8V GPU_IFPX FET



1.8V GPU_IFPX FET	
MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: Power FETs

Apple Inc.

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State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.3V S5 ENABLE

SMC_PM_G2_EN → R7902 100 → P3V3S5_EN
R7958 100K (PLACE_NEAR=U4900.L13:3mm)
C7902 NO STUFF 0.068UF (PLACE_NEAR=R7252.2:2mm)
R7901 100 → P5VS5_EN
C7901 NO STUFF 0.068UF
P3V3S5_PGOOD → R7941 0 → RSMRST_PWRGD
PP3V42_G3H → R7940 100K
OMIT C7941 NOSTUFF

S5 rail PWRGD

Unused PGOOD signal

TP_P1V2S0_PGOOD
TP_GPUIFPX_PGOOD
TP_P1V5S3RS0_PGOOD
TP_GFXIMVP_PGOOD
TP_DDRREG_PGOOD

3.3V,5V S3 ENABLE

PM_SLP_S4_L (PM_S4_STATE_L) PM_SLP_S4_L
R7911 5.1K
R7912 0
PLACE_NEAR=R7251.2:3mm
PLACE_NEAR=U7300.11:3mm
P5VS3_EN
DDRREG_EN
C7910 0.47UF
NO STUFF C7912 0.47UF

S0 ENABLE (PM_SLP_S3_L)

PM_SLP_S3_L → R7978 100
R7979 100K
PM_SLP_S3_L_R
R7981 33K
R7985 10K
R7986 5.1K
PM_SLP_S3_L_R
P1V8S0_EN
P1V2GMUX_EN
CPUVTTS0_EN
C7981 0.47UF
C7985 0.47UF
C7986 0.47UF

Other S0 RAILS

PP3V3_S0
R7992 10K
PM_ALL_GFX_PGOOD
TGL HIGH
EGL PM_ALL_GPU_PGOOD
R7995 100 ← S0PGOOD_PWROK
R7996 100 ← P1V8S0_PGOOD
R7997 100 ← P5VS3_PGOOD → S0_PWR_PGOOD
R7991 100 ← PM_ALL_GPU_PGOOD, ALL_GFX_PGOOD_R
PLACE_NEAR=U7980.1:2mm
PP3V3_S5
R7994 0
C7989 0.1UF
U7980 TC7SZ08AFEAPE SOT665 → ALL_SYS_PWRGD

CHGR VFRQ Generation

VFRQ_SLPS4 R7933 0
VFRQ_SLPS3 R7932 0
PP3V42_G3H
R7931 10K
Q7931 SSM3K15FV SOD-VESM-HF
CHGR_VFRQ
NO STUFF R7935 0
VFRQ_EN_GATE
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

27MHZ OE EN Generation

PP3V3_S0
R7999 10K
Q7995 SSM3K15FV SOD-VESM-HF
CK505_27MHZ_EN_L

EXT GPU PWRGD Pullup

PP3V3_S0
R7990 100K
PM_ALL_GPU_PGOOD
PM_ALL_GPU_PGOOD

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

PP3V3_S0
RAIL_MON
C7971 0.1uF (PLACE_NEAR=U7971.7:2mm)
U7971 ISL88042IRTJJZ TDFN
V2MON
V3MON CRITICAL
V4MON
PP3V3_S0
PP1V5_S0
PPCPUVTT_S0
NC
S0PGOOD_PWROK
V2MON THRESHOLD IS 2.866V
V3MON THRESHOLD IS 0.6V
V4MON THRESHOLD IS 0.6V

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R7920 & Q7920, MUST BE S3 RAIL.

3.3V ENET FET

PP3V3_S3
R7920 10K
R7921 10K
R7922 100K
C7921 0.033UF
C7922 0.01UF
Q7922 CRITICAL NTR4101P SOT-23-HF
PP3V3_ENET
PM_ENET_EN
C7920 0.22UF
Q7921 2N7002DW-X-G SOT-363
PM_ENET_EN_L
P3V3ENET_SS

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_SLP_S3_L
WOL_EN
SMC_ADAPTER_EN
AC_EN_L
(AC_EN_L)
(PM_SLP_S3_L)
Q7920 2N7002DW-X-G SOT-363
Q7925 2N7002DW-X-G SOT-363
PM_WLAN_EN_L
AP_PWR_EN

GPU Rail Sequencing

GT216 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUVcore
4) GDDR3 1.8V

EG_RAIL1_EN
EG_RAIL2_EN
EG_RAIL3_EN
EG_RAIL4_EN

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009
PAGE TITLE: Power Control
Apple Inc.
DRAWING NUMBER: D
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BRANCH:
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEX 1.05V Current = 2A

250mA

1500mA

120 mA: GT216 A01 DG v3 01/09

NC_GPU_DFM
ND_TEST=TRUE

OMIT

U8000
NV-GT216
BGA
(2 OF 9)

PP1V05_S0GPU
PP1V05_S0GPU
PP1V05_S0GPU

PP1V05_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V

L8015 100NH-700MA-0.14OHM 0603

GPU_VDD_SENSE
GPU_GND_SENSE

NC_GPU_BUFRST_L

OMIT

U8000
NV-GT216
BGA
(1 OF 9)

PEG_R2D_C_P<0> C8020 0.1uF PEG_R2D_P<0> AP17 PEX_RX0
PEG_R2D_C_N<0> C8021 0.1uF PEG_R2D_N<0> AN17 PEX_RX0*
PEG_R2D_C_P<1> C8022 0.1uF PEG_R2D_P<1> AN19 PEX_RX1
PEG_R2D_C_N<1> C8023 0.1uF PEG_R2D_N<1> AP19 PEX_RX1*
PEG_R2D_C_P<2> C8024 0.1uF PEG_R2D_P<2> AR19 PEX_RX2
PEG_R2D_C_N<2> C8025 0.1uF PEG_R2D_N<2> AR20 PEX_RX2*
PEG_R2D_C_P<3> C8026 0.1uF PEG_R2D_P<3> AP20 PEX_RX3
PEG_R2D_C_N<3> C8027 0.1uF PEG_R2D_N<3> AN20 PEX_RX3*
PEG_R2D_C_P<4> C8028 0.1uF PEG_R2D_P<4> AN22 PEX_RX4
PEG_R2D_C_N<4> C8029 0.1uF PEG_R2D_N<4> AP22 PEX_RX4*
PEG_R2D_C_P<5> C8030 0.1uF PEG_R2D_P<5> AR22 PEX_RX5
PEG_R2D_C_N<5> C8031 0.1uF PEG_R2D_N<5> AR23 PEX_RX5*
PEG_R2D_C_P<6> C8032 0.1uF PEG_R2D_P<6> AP23 PEX_RX6
PEG_R2D_C_N<6> C8033 0.1uF PEG_R2D_N<6> AN23 PEX_RX6*
PEG_R2D_C_P<7> C8034 0.1uF PEG_R2D_P<7> AN25 PEX_RX7
PEG_R2D_C_N<7> C8035 0.1uF PEG_R2D_N<7> AP25 PEX_RX7*
PEG_R2D_C_P<8> C8036 0.1uF PEG_R2D_P<8> AR25 PEX_RX8
PEG_R2D_C_N<8> C8037 0.1uF PEG_R2D_N<8> AR26 PEX_RX8*
PEG_R2D_C_P<9> C8038 0.1uF PEG_R2D_P<9> AP26 PEX_RX9
PEG_R2D_C_N<9> C8039 0.1uF PEG_R2D_N<9> AN26 PEX_RX9*
PEG_R2D_C_P<10> C8040 0.1uF PEG_R2D_P<10> AN28 PEX_RX10
PEG_R2D_C_N<10> C8041 0.1uF PEG_R2D_N<10> AP28 PEX_RX10*
PEG_R2D_C_P<11> C8042 0.1uF PEG_R2D_P<11> AR28 PEX_RX11
PEG_R2D_C_N<11> C8043 0.1uF PEG_R2D_N<11> AR29 PEX_RX11*
PEG_R2D_C_P<12> C8044 0.1uF PEG_R2D_P<12> AP29 PEX_RX12
PEG_R2D_C_N<12> C8045 0.1uF PEG_R2D_N<12> AN29 PEX_RX12*
PEG_R2D_C_P<13> C8046 0.1uF PEG_R2D_P<13> AN31 PEX_RX13
PEG_R2D_C_N<13> C8047 0.1uF PEG_R2D_N<13> AP31 PEX_RX13*
PEG_R2D_C_P<14> C8048 0.1uF PEG_R2D_P<14> AR31 PEX_RX14
PEG_R2D_C_N<14> C8049 0.1uF PEG_R2D_N<14> AR32 PEX_RX14*
PEG_R2D_C_P<15> C8050 0.1uF PEG_R2D_P<15> AR34 PEX_RX15
PEG_R2D_C_N<15> C8051 0.1uF PEG_R2D_N<15> AP34 PEX_RX15*

PEG_CLK100M_P AR16 PEX_REFCLK
PEG_CLK100M_N AR17 PEX_REFCLK*
EG_RESET_L R8020 0 GPU_RESET_R_L AM16 PEX_RST*
PEX_CLKREQ_L AR13 PEX_CLKREQ*

PP3V3_S0GPU R8021 10K

PP1V05_S0GPU R8012 NO STUFF 0 PP3V3R1V05_GPU_PEX_SVDD
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MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

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PEX_TX0* AM17 PEG_D2R_C_N<0> C8056 0.1uF PEG_D2R_N<0>
PEX_TX1 AM18 PEG_D2R_C_P<1> C8057 0.1uF PEG_D2R_P<1>
PEX_TX1* AM19 PEG_D2R_C_N<1> C8058 0.1uF PEG_D2R_N<1>
PEX_TX2 AL19 PEG_D2R_C_P<2> C8059 0.1uF PEG_D2R_P<2>
PEX_TX2* AK19 PEG_D2R_C_N<2> C8060 0.1uF PEG_D2R_N<2>
PEX_TX3 AL20 PEG_D2R_C_P<3> C8061 0.1uF PEG_D2R_P<3>
PEX_TX3* AM20 PEG_D2R_C_N<3> C8062 0.1uF PEG_D2R_N<3>
PEX_TX4 AM21 PEG_D2R_C_P<4> C8063 0.1uF PEG_D2R_P<4>
PEX_TX4* AM22 PEG_D2R_C_N<4> C8064 0.1uF PEG_D2R_N<4>
PEX_TX5 AL22 PEG_D2R_C_P<5> C8065 0.1uF PEG_D2R_P<5>
PEX_TX5* AK22 PEG_D2R_C_N<5> C8066 0.1uF PEG_D2R_N<5>
PEX_TX6 AL23 PEG_D2R_C_P<6> C8067 0.1uF PEG_D2R_P<6>
PEX_TX6* AM23 PEG_D2R_C_N<6> C8068 0.1uF PEG_D2R_N<6>
PEX_TX7 AM24 PEG_D2R_C_P<7> C8069 0.1uF PEG_D2R_P<7>
PEX_TX7* AM25 PEG_D2R_C_N<7> C8070 0.1uF PEG_D2R_N<7>
PEX_TX8 AL25 PEG_D2R_C_P<8> C8071 0.1uF PEG_D2R_P<8>
PEX_TX8* AK25 PEG_D2R_C_N<8> C8072 0.1uF PEG_D2R_N<8>
PEX_TX9 AL26 PEG_D2R_C_P<9> C8073 0.1uF PEG_D2R_P<9>
PEX_TX9* AM26 PEG_D2R_C_N<9> C8074 0.1uF PEG_D2R_N<9>
PEX_TX10 AM27 PEG_D2R_C_P<10> C8075 0.1uF PEG_D2R_P<10>
PEX_TX10* AM28 PEG_D2R_C_N<10> C8076 0.1uF PEG_D2R_N<10>
PEX_TX11 AL28 PEG_D2R_C_P<11> C8077 0.1uF PEG_D2R_P<11>
PEX_TX11* AK28 PEG_D2R_C_N<11> C8078 0.1uF PEG_D2R_N<11>
PEX_TX12 AK29 PEG_D2R_C_P<12> C8079 0.1uF PEG_D2R_P<12>
PEX_TX12* AL29 PEG_D2R_C_N<12> C8080 0.1uF PEG_D2R_N<12>
PEX_TX13 AM29 PEG_D2R_C_P<13> C8081 0.1uF PEG_D2R_P<13>
PEX_TX13* AM30 PEG_D2R_C_N<13> C8082 0.1uF PEG_D2R_N<13>
PEX_TX14 AN31 PEG_D2R_C_P<14> C8083 0.1uF PEG_D2R_P<14>
PEX_TX14* AM32 PEG_D2R_C_N<14> C8084 0.1uF PEG_D2R_N<14>
PEX_TX15 AN32 PEG_D2R_C_P<15> C8085 0.1uF PEG_D2R_P<15>
PEX_TX15* AP32 PEG_D2R_C_N<15> C8086 0.1uF PEG_D2R_N<15>

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_P NO STUFF R8060 200
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK_N
PEX_TERMP AG21 PEX_TERMP_PD R8050 2.49K
PEX_SVDD_3V3 AG19 F7 C8013 4.7UF C8012 0.1UF

SYNC_MASTER=K18_MLB	SYNC_DATE=06/29/2009
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Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

7 PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 10% 16V X5R 402
C8101 0.22UF 10% 6.3V CERM-X5R 402
C8102 0.22UF 10% 6.3V CERM-X5R 402
C8103 0.1UF 10% 16V X7R-CERM 402
C8104 0.047UF 10% 16V X7R 402
C8105 0.047UF 10% 16V X7R 402
C8106 0.047UF 10% 16V X7R 402
C8107 0.022UF 10% 16V CERM-X5R 402
C8108 0.022UF 10% 16V CERM-X5R 402
C8109 0.022UF 10% 16V CERM-X5R 402
C8110 0.015UF 10% 16V X7R 402
C8111 0.015UF 10% 16V X7R 402
C8112 0.01UF 10% 25V X7R 402
C8113 0.01UF 10% 25V X7R 402
C8114 0.01UF 10% 25V X7R 402
C8115 0.01UF 10% 25V X7R 402
C8116 0.01UF 10% 25V X7R 402
C8117 0.01UF 10% 25V X7R 402
C8118 0.0068UF 10% 25V CERM 402
C8119 0.0047UF 10% 25V CERM 402

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VDD: L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

VDD: V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

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GND: B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

GND: V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AD9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30 K9 AK14

79 78 77 51 8 7 6 PP1V8_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8156 4.7UF 20% 6.3V CERM 603
C8157 0.1UF 10% 16V CERM 402
C8158 0.1UF 10% 16V CERM 402
C8159 0.1UF 10% 16V CERM 402
C8160 0.047UF 10% 16V X7R 402
C8162 0.047UF 10% 16V X7R 402
C8163 0.047UF 10% 16V X7R 402
C8164 0.01UF 10% 25V X7R 402
C8165 0.01UF 10% 25V X7R 402
C8166 0.01UF 10% 25V X7R 402

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FBVDDQ: B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

FBVDDQ: J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

SYNC_MASTER=GT216 SYNC_DATE=03/26/2009

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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FB_A_DQ<0> L32 FBA_D00
FB_A_DQ<1> N33 FBA_D01
FB_A_DQ<2> L33 FBA_D02
FB_A_DQ<3> N34 FBA_D03
FB_A_DQ<4> N35 FBA_D04
FB_A_DQ<5> P35 FBA_D05
FB_A_DQ<6> P33 FBA_D06
FB_A_DQ<7> P34 FBA_D07
FB_A_DQ<8> K35 FBA_D08
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FB_A_DQ<28> M30 FBA_D28
FB_A_DQ<29> P31 FBA_D29
FB_A_DQ<30> R32 FBA_D30
FB_A_DQ<31> R30 FBA_D31
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FB_A_DQ<33> AG32 FBA_D33
FB_A_DQ<34> AH31 FBA_D34
FB_A_DQ<35> AF31 FBA_D35
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FB_A_DQ<57> AE32 FBA_D57
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FB_A_DQ<59> AE35 FBA_D59
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FB_A_DQ<61> AE33 FBA_D61
FB_A_DQ<62> AB32 FBA_D62
FB_A_DQ<63> AC35 FBA_D63

NCX H29
NCX G29
NCX J29
NCX K29
NCX AD29
NCX AE29
NCX AG29
NCX AH29
NC

FBA_CMD0 V32 FB_A_LMA<4>
FBA_CMD1 W31 FB_A_RAS_L
FBA_CMD2 U31 FB_A_LMA<5>
FBA_CMD3 Y32 FB_A_BA<1>
FBA_CMD4 AB35 FB_A_UMA<2>
FBA_CMD5 AB34 FB_A_UMA<4>
FBA_CMD6 W35 FB_A_UMA<3>
FBA_CMD7 W33 FB_A_UCKE
FBA_CMD8 W30 FB_A_UCS0_L
FBA_CMD9 T34 FB_A_MA<11>
FBA_CMD10 T35 FB_A_LCAS_L
FBA_CMD11 AB31 FB_A_WE_L
FBA_CMD12 Y30 FB_A_BA<0>
FBA_CMD13 Y34 FB_A_UMA<5>
FBA_CMD14 W32 FB_A_MA<12>
FBA_CMD15 AA30 FB_A_DRAM_RST
FBA_CMD16 AA32 FB_A_MA<7>
FBA_CMD17 Y33 FB_A_MA<10>
FBA_CMD18 U32 FB_A_LCKE
FBA_CMD19 Y31 FB_A_MA<0>
FBA_CMD20 U34 FB_A_MA<9>
FBA_CMD21 Y35 FB_A_MA<6>
FBA_CMD22 W34 FB_A_LMA<2>
FBA_CMD23 V30 FB_A_MA<8>
FBA_CMD24 U35 FB_A_LMA<3>
FBA_CMD25 U30 FB_A_MA<1>
FBA_CMD26 U33 NC_FBA_MA<13>
FBA_CMD27 AB30 FB_A_BA<2>
FBA_CMD28 AB33 NC_FB_A_UCS1_L
FBA_CMD29 T33 FB_A_LCS0_L
FBA_CMD30 W29 NC_FB_A_LCS1_L

FBA_CLK0 T32 FB_A_CLK_P<0>
FBA_CLK0* T31 FB_A_CLK_N<0>
FBA_CLK1 AC31 FB_A_CLK_P<1>
FBA_CLK1* AC30 FB_A_CLK_N<1>

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FBA_DQM1 H34 FB_A_DQM_L<1>
FBA_DQM2 J30 FB_A_DQM_L<2>
FBA_DQM3 P30 FB_A_DQM_L<3>
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FBA_DQS_RN2 H31 FB_A_RDQS<2>
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FBA_DQS_RN4 AD32 FB_A_RDQS<4>
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MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

FBA_DEBUG T30 FB_A_UCAS_L

FB_CAL_PD_VDDQ K27 FBCAL_PD_VDDQ
FB_CAL_PU_GND L27 FBCAL_PU_GND
FB_CAL_TERM_GND M27 FBCAL_TERM_GND

R8203 1 10K 5% 1/16W MF-LF 402 2
R8200 1 10K 5% 1/16W MF-LF 402 2
R8201 1 10K 5% 1/16W MF-LF 402 2

82 80 75 51 7 6 PP1V05_S0GPU
L8200 FERR-220-OHM-2.5A 0603
C8202 1 1UF 10% 6.3V CERM 402
C8200 1 4.7UF 10% 6.3V X5R-CERM 603
C8201 1 4.7UF 10% 6.3V X5R-CERM 603

79 78 77 76 51 8 7 6 PP1V8_S0GPU_ISNS
R8290 1 56.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.K27:3mm

R8292 1 40.2 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.M27:3mm
R8291 1 31.6 1% 1/16W MF-LF 402 2
PLACE_NEAR=U8000.L27:3mm

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FB_B_DQ<0> B13 FBC_D00
FB_B_DQ<1> D13 FBC_D01
FB_B_DQ<2> A13 FBC_D02
FB_B_DQ<3> A14 FBC_D03
FB_B_DQ<4> C16 FBC_D04
FB_B_DQ<5> B16 FBC_D05
FB_B_DQ<6> A17 FBC_D06
FB_B_DQ<7> D16 FBC_D07
FB_B_DQ<8> C13 FBC_D08
FB_B_DQ<9> B11 FBC_D09
FB_B_DQ<10> C11 FBC_D10
FB_B_DQ<11> A11 FBC_D11
FB_B_DQ<12> C10 FBC_D12
FB_B_DQ<13> C8 FBC_D13
FB_B_DQ<14> B8 FBC_D14
FB_B_DQ<15> A8 FBC_D15
FB_B_DQ<16> F8 FBC_D16
FB_B_DQ<17> F8 FBC_D17
FB_B_DQ<18> F10 FBC_D18
FB_B_DQ<19> F9 FBC_D19
FB_B_DQ<20> F12 FBC_D20
FB_B_DQ<21> D8 FBC_D21
FB_B_DQ<22> D11 FBC_D22
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FB_B_DQ<28> F15 FBC_D28
FB_B_DQ<29> E16 FBC_D29
FB_B_DQ<30> F16 FBC_D30
FB_B_DQ<31> F17 FBC_D31
FB_B_DQ<32> D29 FBC_D32
FB_B_DQ<33> F27 FBC_D33
FB_B_DQ<34> F28 FBC_D34
FB_B_DQ<35> E28 FBC_D35
FB_B_DQ<36> D26 FBC_D36
FB_B_DQ<37> F25 FBC_D37
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FB_B_DQ<39> E25 FBC_D39
FB_B_DQ<40> E32 FBC_D40
FB_B_DQ<41> F32 FBC_D41
FB_B_DQ<42> D33 FBC_D42
FB_B_DQ<43> E31 FBC_D43
FB_B_DQ<44> C33 FBC_D44
FB_B_DQ<45> E29 FBC_D45
FB_B_DQ<46> D30 FBC_D46
FB_B_DQ<47> E29 FBC_D47
FB_B_DQ<48> B29 FBC_D48
FB_B_DQ<49> C31 FBC_D49
FB_B_DQ<50> C29 FBC_D50
FB_B_DQ<51> B31 FBC_D51
FB_B_DQ<52> C32 FBC_D52
FB_B_DQ<53> B32 FBC_D53
FB_B_DQ<54> B35 FBC_D54
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FB_B_DQ<59> C28 FBC_D59
FB_B_DQ<60> C26 FBC_D60
FB_B_DQ<61> D25 FBC_D61
FB_B_DQ<62> B25 FBC_D62
FB_B_DQ<63> A25 FBC_D63

NCX C11
NCX C12
NCX C14
NCX C15
NCX C24
NCX C25
NCX C27
NCX C28
NC

FBC_CMD0 C17 FB_B_LMA<4>
FBC_CMD1 B19 FB_B_RAS_L
FBC_CMD2 D18 FB_B_LMA<5>
FBC_CMD3 F21 FB_B_BA<1>
FBC_CMD4 A23 FB_B_UMA<2>
FBC_CMD5 D21 FB_B_UMA<4>
FBC_CMD6 B23 FB_B_UMA<3>
FBC_CMD7 E20 FB_B_UCKE
FBC_CMD8 G21 FB_B_UCS0_L
FBC_CMD9 F20 FB_B_MA<11>
FBC_CMD10 F19 FB_B_LCAS_L
FBC_CMD11 F23 FB_B_WE_L
FBC_CMD12 A22 FB_B_BA<0>
FBC_CMD13 C22 FB_B_UMA<5>
FBC_CMD14 B17 FB_B_MA<12>
FBC_CMD15 F24 FB_B_DRAM_RST
FBC_CMD16 C25 FB_B_MA<7>
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FBC_CMD27 F22 FB_B_BA<2>
FBC_CMD28 C23 NC_FB_B_UCS1_L
FBC_CMD29 B20 FB_B_LCS0_L
FBC_CMD30 A20 NC_FB_B_LCS1_L

FBC_CLK0 E17 FB_B_CLK_P<0>
FBC_CLK0* D17 FB_B_CLK_N<0>
FBC_CLK1 D23 FB_B_CLK_P<1>
FBC_CLK1* E23 FB_B_CLK_N<1>

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FBC_DQM1 D10 FB_B_DQM_L<1>
FBC_DQM2 F11 FB_B_DQM_L<2>
FBC_DQM3 D15 FB_B_DQM_L<3>
FBC_DQM4 D27 FB_B_DQM_L<4>
FBC_DQM5 D34 FB_B_DQM_L<5>
FBC_DQM6 A34 FB_B_DQM_L<6>
FBC_DQM7 D28 FB_B_DQM_L<7>

FBC_DQS_RN0 B14 FB_B_RDQS<0>
FBC_DQS_RN1 B10 FB_B_RDQS<1>
FBC_DQS_RN2 D9 FB_B_RDQS<2>
FBC_DQS_RN3 E14 FB_B_RDQS<3>
FBC_DQS_RN4 F26 FB_B_RDQS<4>
FBC_DQS_RN5 D31 FB_B_RDQS<5>
FBC_DQS_RN6 A31 FB_B_RDQS<6>
FBC_DQS_RN7 A26 FB_B_RDQS<7>

FBC_DQS_WP0 C14 FB_B_WDQS<0>
FBC_DQS_WP1 A10 FB_B_WDQS<1>
FBC_DQS_WP2 E10 FB_B_WDQS<2>
FBC_DQS_WP3 D14 FB_B_WDQS<3>
FBC_DQS_WP4 E26 FB_B_WDQS<4>
FBC_DQS_WP5 D32 FB_B_WDQS<5>
FBC_DQS_WP6 A32 FB_B_WDQS<6>
FBC_DQS_WP7 B26 FB_B_WDQS<7>

FBC_DEBUG G19 FB_B_UCAS_L
FB_VREF J27 GPU_FB_VREF

R8252 1 10K 5% 1/16W MF-LF 402 2
R8251 1 10K 5% 1/16W MF-LF 402 2
R8250 1 10K 5% 1/16W MF-LF 402 2

79 51 8 7 6 PP1V8_S0GPU_ISNS
R8295 1 1.07K 1% 1/16W MF-LF 402 2

NO STUFF
C8296 1 0.1UF 10% 10V X5R 2 402
R8297 1 1.02K 1% 1/16W MF-LF 402 2
R8296 1 2.49K 1% 1/16W MF-LF 402 2

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
NO STUFF GPU_FB_VREF_UNTERM_L
Q8295 SSM6N15FEAPE SOT563
81 80 79 78 FB_VREF_UNTERM

NO STUFF
Q8295 SSM6N15FEAPE SOT563
NC NC NC NC

SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009
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NV GT216 FRAME BUFFER I/F
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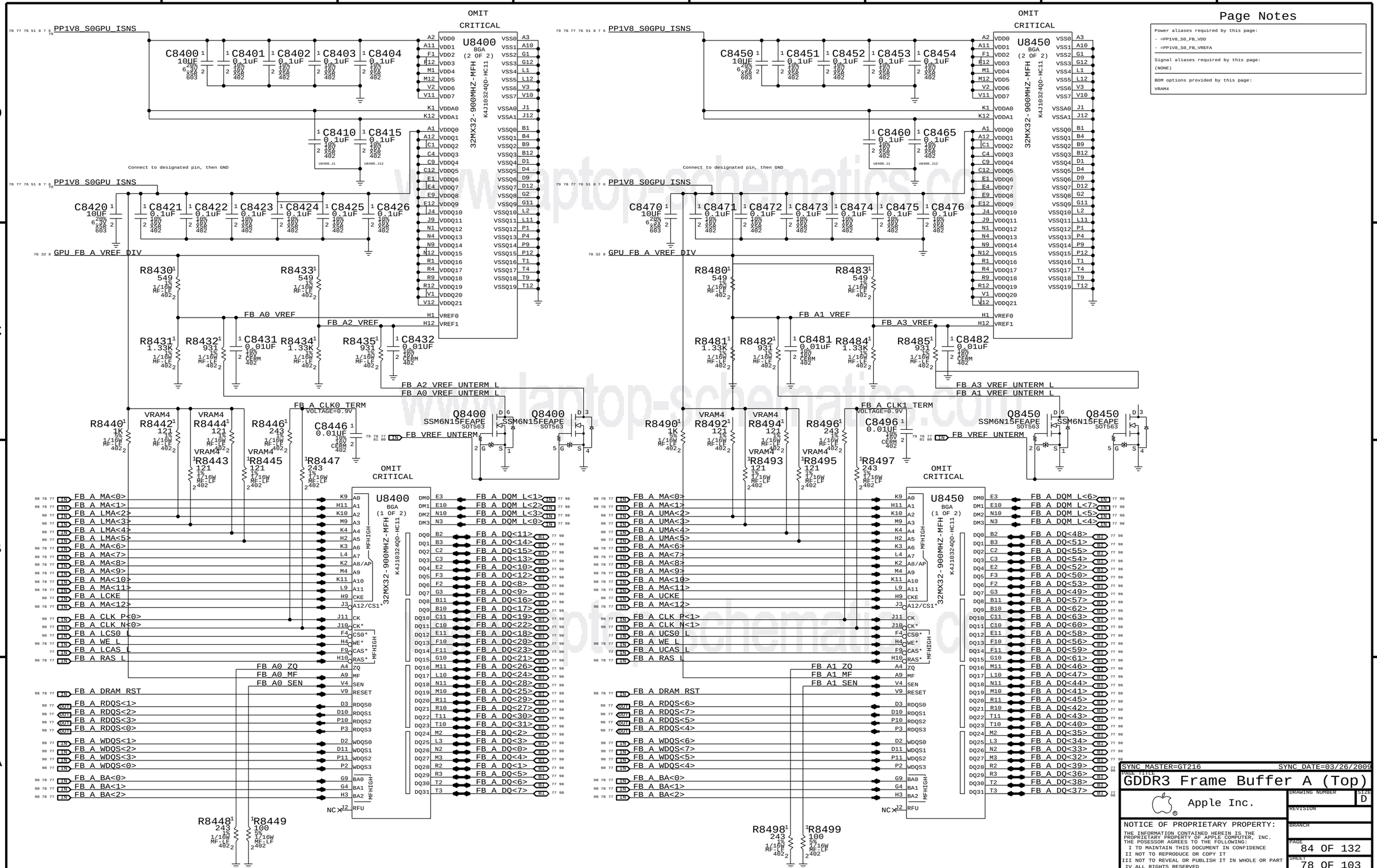

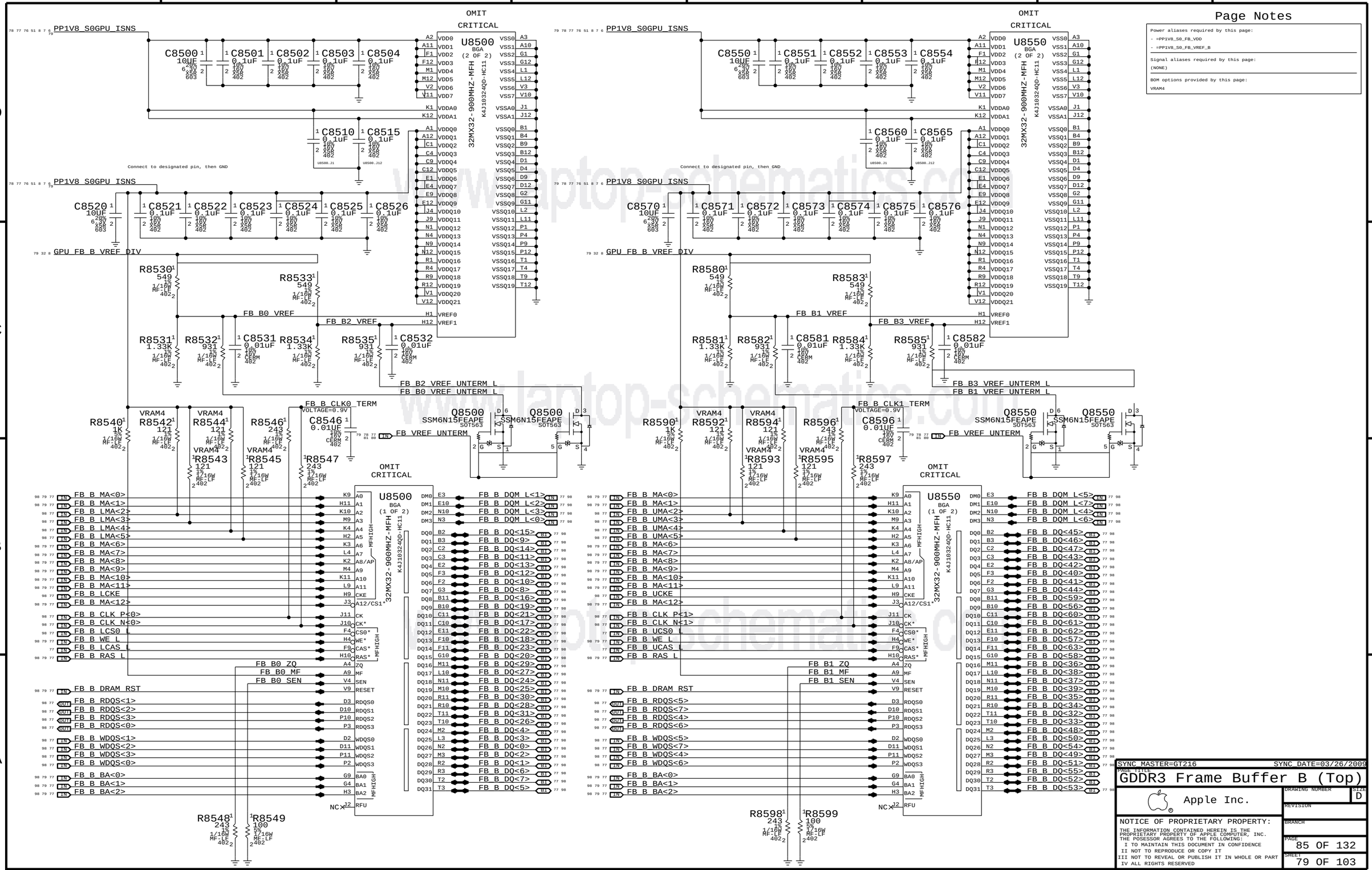

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

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PP3V3_S0GPU
C8694 0.1UF 20% 10V CERM 402
C8696 1UF 10% 6.3V X5R 402
C8698 4.7UF 20% 6.3V X5R-CERM1 402
J9 J10 J11 J12 J13 VDD33

NC_GPU_ROM_CS_L C3 ROM_CS*
GPU_ROM_SCLK D4 ROM_SCLK
GPU_ROM_SI D3 ROM_SI
GPU_ROM_SO C4 ROM_SO
R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402
GPU_STRAP_REF_3V3_PD N9 MULTI_STRAP_REF0_GND
GPU_STRAP_REF_MIOB_PD P9 MULTI_STRAP_REF1_GND

PP3V3_S0GPU
R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1UF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402
P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

GPU_TESTMODE_PD AP35 TESTMODE
GPU_MIOA_VREF N5 MIOA_VREF
GPU_MIOB_VREF AF1 MIOB_VREF
GPU_MIOA_PD_VDDQ U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND AA6 MIOB_CAL_PU_GND

AF9 SP_PLLVDD
65mA AE9 PLLVDD
AD9 VID_PLLVDD

PP1V05_S0GPU
L8635 100NH-700MA-0.14OHM 0603
PP1V05_GPU_H_PLLVDD_F 25mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 1UF 10% 6.3V X5R 402

PP1V05_S0GPU
L8640 100NH-700MA-0.14OHM 0603
PP1V05_GPU_VID_PLLVDD_F 50mA
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 1UF 10% 6.3V X5R 402
C8631 0.1UF 10% 16V X5R 402

GPU_CLK27M B1 XTAL_IN
NC_GPU_XTALOUT B2 XTAL_OUT
GPU_XTALOUTBUFF D1 XTAL_OUTBUFF
GPU_CLK27M_SS D2 XTAL_SSIN

GPU_STRAP<0> W5 STRAP0
GPU_STRAP<1> W7 STRAP1
GPU_STRAP<2> V7 STRAP2

GPIO0	K1	GPU_VCORE_VID3	B3
GPIO1	K2	DP_EG_HPD	B3
GPIO2	K3	GPU_VCORE_VID4	B3
GPIO3	H3	EG_LCD_PWR_EN	B3
GPIO4	H2	EG_BKLT_EN	B3
GPIO5	H1	GPU_VCORE_VID0	B3
GPIO6	H4	GPU_VCORE_VID1	B3
GPIO7	H5	GPU_VCORE_VID2	B3
GPIO8	H6	SMC_GFX_OVERTEMP_R	B3
GPIO9	J7	TP_GPU_GSTATE<0>	B3
GPIO10	K4	FB_VREF_UNTERM	B3
GPIO11	K5	GPU_GPIO_11	B3
GPIO12	H7	SMC_GFX_THROTTLE_R	B3
GPIO13	J4	FBVDD_ALTVO	B3
GPIO14	J6	NC_GPU_GPIO_14	B3
GPIO15	L1	NC_GPU_GPIO_15	B3
GPIO16	L2	GPU_GPIO_16	B3
GPIO17	L4	NC_GPU_GPIO_17	B3
GPIO18	M4	NC_GPU_GPIO_18	B3
GPIO19	L7	NC_GPU_GPIO_19	B3
GPIO20	L5	NC_GPU_GPIO_20	B3
GPIO21	K6	NC_GPU_GPIO_21	B3
GPIO22	L6	NC_GPU_GPIO_22	B3
GPIO23	M6	NC_GPU_GPIO_23	B3

JTAG_TCK	AP14	TP_GPU_JTAG_TCK	IN
JTAG_TDI	AN14	TP_GPU_JTAG_TDI	IN
JTAG_TDO	AN16	TP_GPU_JTAG_TDO	OUT
JTAG_TMS	AR14	TP_GPU_JTAG_TMS	IN
JTAG_TRST*	AP16	TP_GPU_JTAG_TRST_L	IN
MIOA_CLKIN	N4	NC_GPU_MIOA_CLKIN	IN
MIOA_CLKOUT	R4	NC_GPU_MIOA_CLKOUT	B3
MIOA_CLKOUT*	T4	NC_GPU_MIOA_CLKOUT_L	B3
MIOA_CTL3	P5	NC_GPU_MIOA_CTL3	B3
MIOA_DE	N2	TP_GPU_MIOA_DE	B3
MIOA_D0	N1	TP_GPU_MIOA_D<0>	B3
MIOA_D1	P4	TP_GPU_MIOA_D<1>	B3
MIOA_D2	P1	TP_GPU_MIOA_D<2>	B3
MIOA_D3	P2	TP_GPU_MIOA_D<3>	B3
MIOA_D4	P3	TP_GPU_MIOA_D<4>	B3
MIOA_D5	T3	TP_GPU_MIOA_D<5>	B3
MIOA_D6	T2	TP_GPU_MIOA_D<6>	B3
MIOA_D7	T1	TP_GPU_MIOA_D<7>	B3
MIOA_D8	U4	TP_GPU_MIOA_D<8>	B3
MIOA_D9	U1	TP_GPU_MIOA_D<9>	B3
MIOA_D10	U2	GPU_MIOA_D<10>	B3
MIOA_D11	U3	GPU_MIOA_D<11>	B3
MIOA_D12	R6	GPU_MIOA_D<12>	B3
MIOA_D13	T6	GPU_MIOA_D<13>	B3
MIOA_D14	N6	GPU_MIOA_D<14>	B3
MIOA_HSYNC	N3	NC_GPU_MIOA_HSYNC	B3
MIOA_VSYNC	L3	NC_GPU_MIOA_VSYNC	B3
MIOB_CLKIN	AE1	NC_GPU_MIOB_CLKIN	IN
MIOB_CLKOUT	V4	NC_GPU_MIOB_CLKOUT	B3
MIOB_CLKOUT*	W4	NC_GPU_MIOB_CLKOUT_L	B3
MIOB_CTL3	W3	NC_GPU_MIOB_CTL3	B3
MIOB_DE	Y5	NC_GPU_MIOB_DE	B3
MIOB_D0	Y1	NC_GPU_MIOB_D<0>	B3
MIOB_D1	Y2	NC_GPU_MIOB_D<1>	B3
MIOB_D2	Y3	NC_GPU_MIOB_D<2>	B3
MIOB_D3	AB3	NC_GPU_MIOB_D<3>	B3
MIOB_D4	AB2	NC_GPU_MIOB_D<4>	B3
MIOB_D5	AB1	NC_GPU_MIOB_D<5>	B3
MIOB_D6	AC4	NC_GPU_MIOB_D<6>	B3
MIOB_D7	AC1	NC_GPU_MIOB_D<7>	B3
MIOB_D8	AC2	NC_GPU_MIOB_D<8>	B3
MIOB_D9	AC3	NC_GPU_MIOB_D<9>	B3
MIOB_D10	AE3	NC_GPU_MIOB_D<10>	B3
MIOB_D11	AE2	NC_GPU_MIOB_D<11>	B3
MIOB_D12	U6	NC_GPU_MIOB_D<12>	B3
MIOB_D13	W6	NC_GPU_MIOB_D<13>	B3
MIOB_D14	Y6	NC_GPU_MIOB_D<14>	B3
MIOB_HSYNC	W1	NC_GPU_MIOB_HSYNC	B3
MIOB_VSYNC	W2	NC_GPU_MIOB_VSYNC	B3
THERMDP	B5	GPU_TDIODE_P	1MM
THERMDN	B4	GPU_TDIODE_N	1MM

SYNC_MASTER=K18_MLB SYNC_DATE=06/29/2009

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NV GT216 GPIO/MIO/MISC

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GPIOs

GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE	OUT	80 81 83
DP_EG_HPD	HPDC	DP_EG_HPD	MAKE_BASE=TRUE	IN	80 81 85
GPU_VCORE_VID4	LCD0_BL_PWM	GPU_VCORE_VID4	MAKE_BASE=TRUE	OUT	80 81 83
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE		80 81 88
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE		80 81 88
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0	MAKE_BASE=TRUE	OUT	80 81 83
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1	MAKE_BASE=TRUE	OUT	80 81 83
GPU_VCORE_VID2	VID2/MEM_VID	GPU_VCORE_VID2	MAKE_BASE=TRUE	OUT	80 81 83
SMC_GFX_OVERTEMP_R_L	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE		80 81
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE		6 80 81
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE		77 78 79 80 81
GPU_GPIO_11	SLI_SYNC	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	OUT	6
SMC_GFX_THROTTLE_R_L	PWR_CTL	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	OUT	80 81
FBVDD_ALTVO	PWR_CTL0	FBVDD_ALTVO	MAKE_BASE=TRUE	OUT	80 81 87
NC_GPU_GPIO_14	PWR_CTL1	NC_GPU_GPIO_14	MAKE_BASE=TRUE NO_TEST=TRUE		80 81

GPIOs

NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET			80 81
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE NO_TEST=TRUE		80 81
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE		80 81

Renamed signals

GPU_CLK27M	MAKE_BASE=TRUE	GPU_CLK27M	27 80 81 98
GPU_CLK27M_SS	MAKE_BASE=TRUE	GPU_CLK27M_SS	80 81 98
GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_TDIODE_P	52 80 81 99
GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_TDIODE_N	52 80 81 99
LVDS_EG_DDC_CLK	MAKE_BASE=TRUE	LVDS_EG_DDC_CLK	81 82 85
LVDS_EG_DDC_DATA	MAKE_BASE=TRUE	LVDS_EG_DDC_DATA	81 82 85
DP_EG_DDC_CLK	MAKE_BASE=TRUE	DP_EG_DDC_CLK	81 82 85
DP_EG_DDC_DATA	MAKE_BASE=TRUE	DP_EG_DDC_DATA	81 82 85

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK	80 81
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI	80 81
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO	80 81
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS	80 81
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L	80 81
NC_FBA_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FBA_MA<13>	77 81
NC_FBB_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FBB_MA<13>	77 81

Unused I2C Buses

NC_GPU_I2CC_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_I2CC_SCL	81 82
NC_GPU_I2CC_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_I2CC_SDA	81 82
NC_GPU_I2CH_SCL	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_I2CH_SCL	81 82
NC_GPU_I2CH_SDA	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_I2CH_SDA	81 82

I2C5 ties into SMBus connection page
(I2C5 requires pullups even if not used)

NC_FB_B_UCS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_B_UCS1_L	77 81
NC_FB_B_LCS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_B_LCS1_L	77 81
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_ROM_CS_L	80 81
NC_FB_A_UCS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_A_UCS1_L	77 81
NC_FB_A_LCS1_L	MAKE_BASE=TRUE NO_TEST=TRUE	NC_FB_A_LCS1_L	77 81
TP_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	TP_LVDS_EG_B_CLK_P	6 81 82
TP_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	TP_LVDS_EG_B_CLK_N	6 81 82
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>	81 82 98
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>	81 82 98
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>	81 82 98
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>	81 82 98

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUTP	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_CLKOUTP	80 81
NC_GPU_MIOA_CLKOUTN	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_CLKOUTN	80 81
NC_GPU_MIOA_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_CTL3	80 81
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	TP_GPU_MIOA_DE	6 80 81
TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	GPU_MIOA_D<9..0>	
NC_GPU_MIOA_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_CLKIN	80 81
NC_GPU_MIOA_D<14..10>	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOA_D<14..10>	80
NC_GPU_MIOA_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_HSYNC	80 81
NC_GPU_MIOA_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOA_VSYNC	80 81
NC_GPU_MIOB_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_CLKIN	80 81
NC_GPU_MIOB_CLKOUTP	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_CLKOUTP	80 81
NC_GPU_MIOB_CLKOUTN	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_CLKOUTN	80 81
NC_GPU_MIOB_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_CTL3	80 81
NC_GPU_MIOB_DE	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_DE	80 81
NC_GPU_MIOB_D<14..0>	MAKE_BASE=TRUE NO_TEST=TRUE	GPU_MIOB_D<14..0>	
NC_GPU_MIOB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_VSYNC	80 81
NC_GPU_MIOB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE	NC_GPU_MIOB_HSYNC	80 81

Config Straps

PP3V3_S0GPU

R8701	45.3K 1% 1/16W MF-LF 402	GPU_STRAP<0>	BI
R8703	34.8K 1% 1/16W MF-LF 402	GPU_STRAP<1>	BI
R8705	10K 1% 1/16W MF-LF 402	GPU_STRAP<2>	BI
R8702	NO STUFF 2.0K 5% 1/16W MF-LF 402		
R8704	NO STUFF 10K 1% 1/16W MF-LF 402		
R8706	NO STUFF 24.9K 1% 1/16W MF-LF 402		

Physical

Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

PP3V3_S0GPU

R8742	100K 1% 1/16W MF-LF 402		
R8743	0 5% 1/16W MF 402		
Q8742	DP_CA_DET_EG_FET, SOD-VESM-HF, SSM3K15FV		

DP_CA_DET_EG_PLD

PP3V3_S0GPU

R8708	OMIT 45.3K 1% 1/16W MF-LF 402	GPU_ROM_SI	OUT
R8709	NO STUFF 4.99K 1% 1/16W MF-LF 402	GPU_ROM_SO	IN
R8711	NO STUFF 15.0K 1% 1/16W MF-LF 402	GPU_ROM_SCLK	IN
R8710	OMIT 10K 1% 1/16W MF-LF 402		
R8712	OMIT 15.0K 1% 1/16W MF-LF 402		

Strap S1/S2 Bit[3:0]	PU/PD	Rval
0 0000	PD	5k
1 0001	PD	10k
2 0010	PD	15k
3 0011	PD	20k
4 0100	PD	25k
5 0101	PD	30k
6 0110	PD	35k
7 0111	PD	45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8 1000	PU	5k
9 1001	PU	10k
A 1010	PU	15k
B 1011	PU	20k
C 1100	PU	25k
D 1101	PU	30k
E 1110	PU	35k
F 1111	PU	45k

PCI_DEVID[4:0]=0x14

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX

PP3V3_S0

PP3V3_S0GPU

R8750	2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_CLK	IN
R8751	2.2K 5% 1/16W MF-LF 402	DP_EG_DDC_DATA	BI
R8752	4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_CLK	IN
R8753	4.7K 5% 1/16W MF-LF 402	DP_IG_DDC_DATA	BI

PP3V3_S0GPU

R8796	2.2K 5% 1/16W MF-LF 402		
R8797	2.2K 5% 1/16W MF-LF 402		
R8798	0 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_R_L	OUT
R8799	0 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_R_L	OUT
		EG_LCD_PWR_EN	OUT
		EG_BKLT_EN	OUT
		FBVDD_ALTVO	OUT
		FB_VREF_UNTERM	OUT
R8792	10K 5% 1/16W MF-LF 402		
R8793	10K 5% 1/16W MF-LF 402		
R8794	10K 5% 1/16W MF-LF 402		
R8795	NO STUFF 10K 5% 1/16W MF-LF 402		

Unused Clocks

R8780	10K 5% 1/16W MF-LF 402	GPU_CLK27M_SS	98 81 80
R8781	10K 5% 1/16W MF-LF 402	GPU_XTALOUTBUFF	80

Isolation FETs for DP MUX inputs

SYNC_MASTER=K18_MLB SYNC_DATE=07/01/2009

PAGE TITLE

GT216 GPIOS & STRAPS

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

PP1V8_GPUIFPX

L8800 FERR-220-OHM-2.5A 0603
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
?mA peak per diff pair
?mA peak for all pairs
Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

PP1V05_S0GPU

L8805 180-OHM-1.5A 0603
C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 10% 6.3V CERM 402
80mA peak

PP1V05_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

GPU_IFPEF_RSET
GPU_IFPC_RSET
GPU_IFPAB_RSET
GPU_IFPD_RSET

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402
R8858 1K 1% 1/16W MF-LF 402

L8810 180-OHM-1.5A 0603
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
?mA peak per diff pair
?mA peak for all pairs
Place at AJ8
Place at AK8

PP1V05_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM-2.5A 0603
C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 10% 6.3V CERM 402
160mA peak

PP3V3_GPU_IFPC_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP3V3_S0GPU

PP1V05_GPU_IFPEF_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V

PP1V8_GPU_IFPEF_PLLVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V
Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

GPU_IFPD_RSET

OMIT

U8000 NV-GT216 BGA (5 OF 9)

AG9	IFPA_IOVDD	IFPA_TXC	AM11	LVDS_EG_A_CLK_P	OUT 88 98
AG10	IFPB_IOVDD	IFPA_TXC*	AM12	LVDS_EG_A_CLK_N	OUT 88 98
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8	LVDS_EG_A_DATA_P<0>	OUT 88 98
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8	LVDS_EG_A_DATA_N<0>	OUT 88 98
AE7	IFPE_IOVDD	IFPA_TXD1	AM10	LVDS_EG_A_DATA_P<1>	OUT 88 98
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9	LVDS_EG_A_DATA_N<1>	OUT 88 98
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10	LVDS_EG_A_DATA_P<2>	OUT 88 98
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10	LVDS_EG_A_DATA_N<2>	OUT 88 98
AJ9	IFPC_PLLVDD	IFPA_TXD3	AK11	NC_LVDS_EG_A_DATA_P<3>	OUT 81 98
AK7	IFPC_RSET	IFPA_TXD3*	AL11	NC_LVDS_EG_A_DATA_N<3>	OUT 81 98
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13	TP_LVDS_EG_B_CLK_P	OUT 6 81
AL1	IFPEF_RSET	IFPB_TXC*	AN13	TP_LVDS_EG_B_CLK_N	OUT 6 81
		IFPB_TXD4	AN8	LVDS_EG_B_DATA_P<0>	OUT 88 98
		IFPB_TXD4*	AP8	LVDS_EG_B_DATA_N<0>	OUT 88 98
		IFPB_TXD5	AP10	LVDS_EG_B_DATA_P<1>	OUT 88 98
		IFPB_TXD5*	AN10	LVDS_EG_B_DATA_N<1>	OUT 88 98
		IFPB_TXD6	AR11	LVDS_EG_B_DATA_P<2>	OUT 88 98
		IFPB_TXD6*	AR10	LVDS_EG_B_DATA_N<2>	OUT 88 98
		IFPB_TXD7	AN11	NC_LVDS_EG_B_DATA_P<3>	OUT 81 98
		IFPB_TXD7*	AP11	NC_LVDS_EG_B_DATA_N<3>	OUT 81 98
		IFPC_AUX_I2CW_SCL	AP2	DP_EG_AUX_CH_P	OUT 85 98
		IFPC_AUX_I2CW_SDA*	AN3	DP_EG_AUX_CH_N	OUT 85 98
		IFPC_L0	AM7	DP_EG_ML_P<0>	OUT 85 98
		IFPC_L0*	AM6	DP_EG_ML_N<0>	OUT 85 98
		IFPC_L1	AL5	DP_EG_ML_P<1>	OUT 85 98
		IFPC_L1*	AM5	DP_EG_ML_N<1>	OUT 85 98
		IFPC_L2	AM3	DP_EG_ML_P<2>	OUT 85 98
		IFPC_L2*	AM4	DP_EG_ML_N<2>	OUT 85 98
		IFPC_L3	AP1	DP_EG_ML_P<3>	OUT 85 98
		IFPC_L3*	AR2	DP_EG_ML_N<3>	OUT 85 98
		IFPD_AUX_I2CX_SCL	AP4	NC	
		IFPD_AUX_I2CX_SDA*	AN4	NC	
		IFPD_L0	AP6	NC	
		IFPD_L0*	AP7	NC	
		IFPD_L1	AP5	NC	
		IFPD_L1*	AN7	NC	
		IFPD_L2	AN5	NC	
		IFPD_L2*	AR5	NC	
		IFPD_L3	AR6	NC	
		IFPD_L3*	AR7	NC	
		IFPE_AUX_I2CY_SCL	AE4	NC	
		IFPE_AUX_I2CY_SDA*	AD4	NC	
		IFPE_L0	AH6	NC	
		IFPE_L0*	AH5	NC	
		IFPE_L1	AH4	NC	
		IFPE_L1*	AG4	NC	
		IFPE_L2	AE5	NC	
		IFPE_L2*	AE6	NC	
		IFPE_L3	AF6	NC	
		IFPE_L3*	AF5	NC	
		IFPF_AUX_I2CZ_SCL	AF3	NC	
		IFPF_AUX_I2CZ_SDA*	AE3	NC	
		IFPF_L0	AL2	NC	
		IFPF_L0*	AL3	NC	
		IFPF_L1	AJ3	NC	
		IFPF_L1*	AJ2	NC	
		IFPF_L2	AJ1	NC	
		IFPF_L2*	AH1	NC	
		IFPF_L3	AH2	NC	
		IFPF_L3*	AH3	NC	
AJ12	DACA_VDD	DACA_RED	AK15	NC	
		DACA_GREEN	AK14	NC	
		DACA_BLUE	AL14	NC	
NC AK12	DACA_VREF	DACA_HSYNC	AM13	NC	
NC AK13	DACA_RSET	DACA_VSYNC	AL13	NC	
AG7	DACB_VDD	DACB_RED	AK7	NC	
		DACB_GREEN	AL7	NC	
		DACB_BLUE	AJ7	NC	
NC AK6	DACB_VREF				
NC AK7	DACB_RSET	CEC	AR5	NC	
AC6	IFPD_PLLVDD				
		DACB_HSYNC	AM2	NC	
AB6	IFPD_RSET	DACB_VSYNC	AM1	NC	

I2C_SCL
I2C_SDA
I2CS_SCL
I2CS_SDA
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA

LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA
NC_GPU_I2CC_SCL
NC_GPU_I2CC_SDA
SMBUS_SMC_0_S5_SCL
SMBUS_SMC_0_S5_SDA
NC_GPU_I2CH_SDA
NC_GPU_I2CH_SCL
DP_EG_DDC_CLK
DP_EG_DDC_DATA

NO STUFF R8861 1K 5% 1/10W MF-LF 402
NO STUFF R8860 1K 5% 1/10W MF-LF 402

SYNC_MASTER=K18_MLB
SYNC_DATE=06/29/2009
PAGE TITLE
NV GT216 VIDEO INTERFACES
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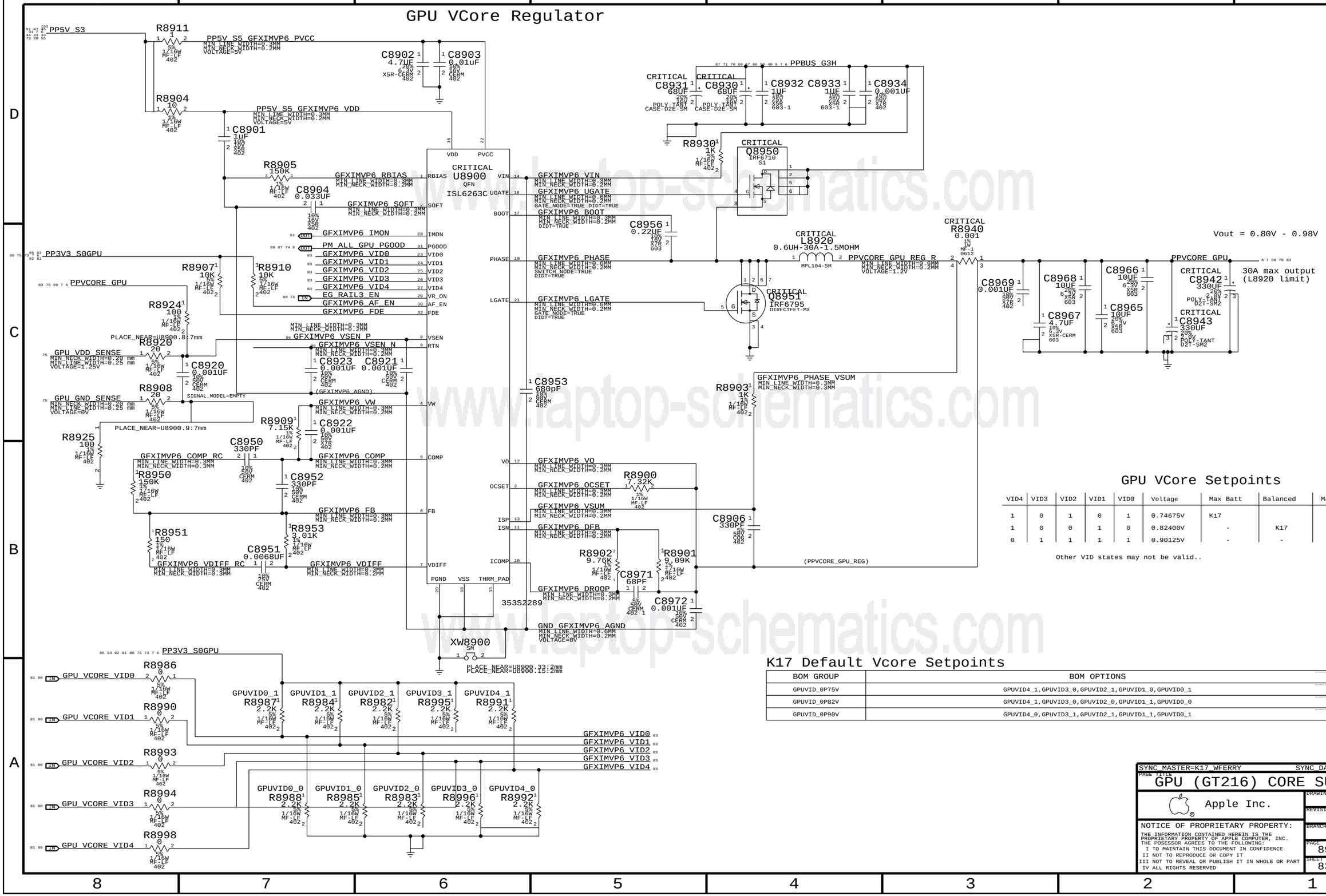
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K17		-
1	0	0	1	0	0.82400V	-	K17	-
0	1	1	1	1	0.90125V	-	-	K17

Other VID states may not be valid..

K17 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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GPU (GT216) CORE SUPPLY

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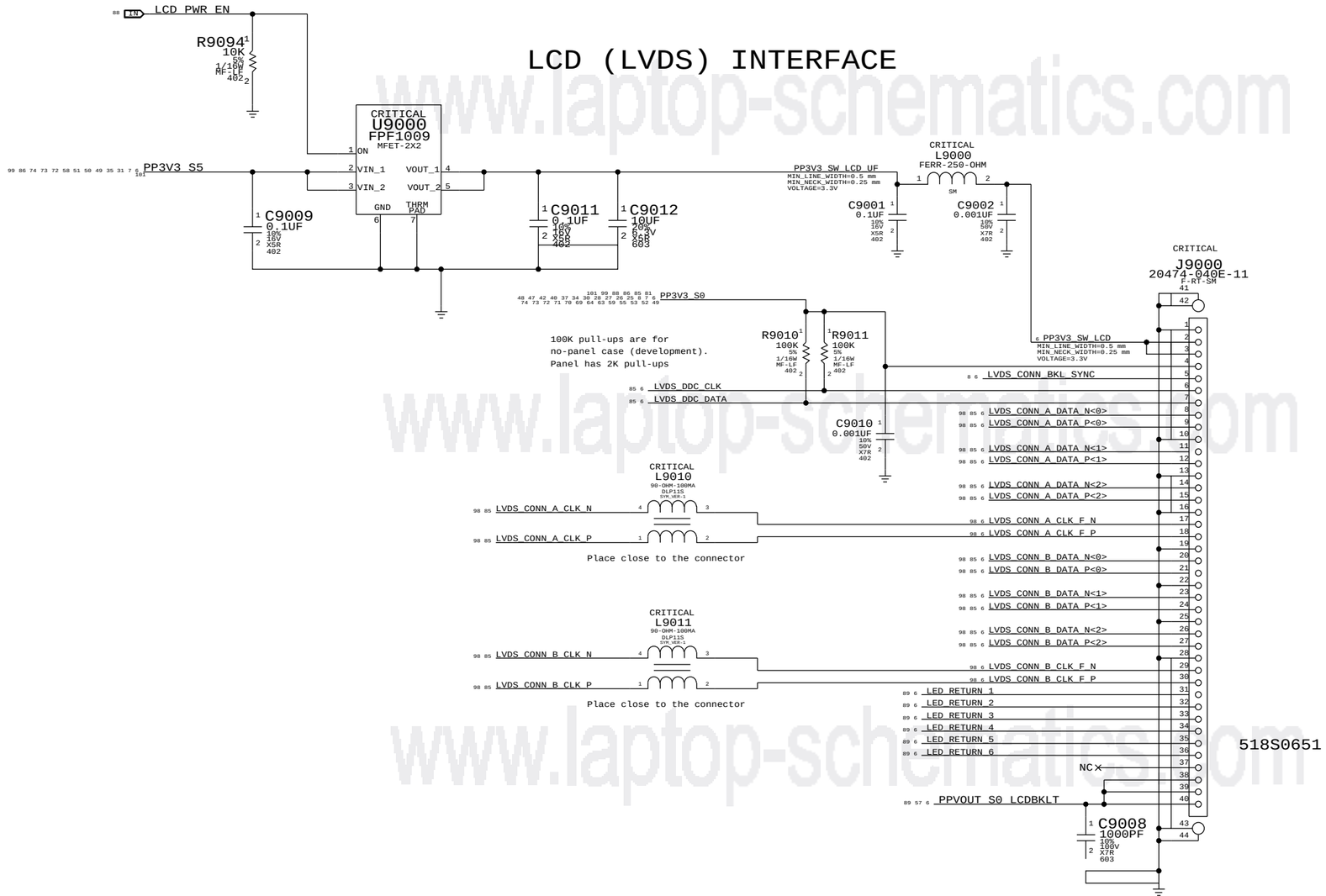
LCD (LVDS) INTERFACE



SYNC_MASTER=K20A_MLB	SYNC_DATE=03/26/2009
PAGE TITLE: LVDS Display Connector	
Apple Inc.	DRAWING NUMBER: SIZE D
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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9320 357 1% 1/10W MF-LF 402
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9322 357 1% 1/10W MF-LF 402
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

R9325 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>
PLACE_NEAR=U9600.A8:7mm

PLACE_NEAR=U9600.B9:7mm
R9327 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

R9330 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>
PLACE_NEAR=U9600.A9:7mm

PLACE_NEAR=U9600.C10:7mm
R9332 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

R9335 357 1% 1/10W MF-LF 402
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>
PLACE_NEAR=U9600.B10:7mm

PLACE_NEAR=U9600.A10:7mm
R9337 357 1% 1/10W MF-LF 402
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

R9340 357 1% 1/10W MF-LF 402
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P
PLACE_NEAR=U9600.C8:7mm

PLACE_NEAR=U9600.C9:7mm
R9342 357 1% 1/10W MF-LF 402
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

R9345 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>
PLACE_NEAR=U9600.A2:7mm

PLACE_NEAR=U9600.A3:7mm
R9347 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

R9350 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>
PLACE_NEAR=U9600.A1:7mm

PLACE_NEAR=U9600.B3:7mm
R9352 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

R9355 357 1% 1/10W MF-LF 402
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>
PLACE_NEAR=U9600.C5:7mm

R9357 357 1% 1/10W MF-LF 402
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>
PLACE_NEAR=U9600.A5:7mm

DisplayPort Mux

PP3V3_S0

U9320 CBTL06141EE BGA CRITICAL

DP_IG_ML_P<0>	B4 DIN1_0+	DOUT_0+ B2 → DP_ML_P<0>
DP_IG_ML_N<0>	A4 DIN1_0-	DOUT_0- B1 → DP_ML_N<0>
DP_IG_ML_P<1>	B5 DIN1_1+	DOUT_1+ D2 → DP_ML_P<1>
DP_IG_ML_N<1>	A5 DIN1_1-	DOUT_1- D1 → DP_ML_N<1>
DP_IG_ML_P<2>	B6 DIN1_2+	DOUT_2+ E2 → DP_ML_P<2>
DP_IG_ML_N<2>	A6 DIN1_2-	DOUT_2- E1 → DP_ML_N<2>
DP_IG_ML_P<3>	A8 DIN1_3+	DOUT_3+ F2 → DP_ML_P<3>
DP_IG_ML_N<3>	A9 DIN1_3-	DOUT_3- F1 → DP_ML_N<3>
DP_IG_AUX_CH_P	H9 DAUX1+	AUX+ H2 → DP_AUX_CH_C_P
DP_IG_AUX_CH_N	J9 DAUX1-	AUX- H1 → DP_AUX_CH_C_N
DP_IG_DDC_CLK	H8 DDC_CLK1	
DP_IG_DDC_DATA	J8 DDC_DAT1	
DP_IG_HPD	J2 HPD_1	
DP_EG_ML_P<0>	B8 DIN2_0+	
DP_EG_ML_N<0>	B9 DIN2_0-	
DP_EG_ML_P<1>	D8 DIN2_1+	
DP_EG_ML_N<1>	D9 DIN2_1-	
DP_EG_ML_P<2>	E8 DIN2_2+	
DP_EG_ML_N<2>	E9 DIN2_2-	
DP_EG_ML_P<3>	F8 DIN2_3+	
DP_EG_ML_N<3>	F9 DIN2_3-	
DP_EG_AUX_CH_P	H6 DAUX2+	
DP_EG_AUX_CH_N	J6 DAUX2-	
DP_EG_DDC_CLK	H5 DDC_CLK2	
DP_EG_DDC_DATA	J5 DDC_DAT2	
DP_EG_HPD	H3 HPD_2	
DP_MUX_SEL_EG	A1 GPU_SEL	DDC_AUX_SEL C2 ← DP_CA_DET
DP_MUX_XSD_L	B7 XSD*	TST0 G2
		HPDIN J1 ← DP_HPD_R

LO=PORT1 HI=PORT2
LO=AUX_CH HI=DDC
PLACE_NEAR=U9320.J1:3mm

C9320 0.1UF 20% 16V CERM 402
C9321 0.1UF 20% 16V CERM 402
C9330 0.1uF 10% 16V X5R 402 (DP_IG_AUX_CH_C_P)
C9331 0.1uF 10% 16V X5R 402 (DP_IG_AUX_CH_C_N)
C9335 0.1uF 10% 16V X5R 402 (DP_EG_AUX_CH_C_P)
C9336 0.1uF 10% 16V X5R 402 (DP_EG_AUX_CH_C_N)

R9304 100K 5% 1/16W MF-LF 402 (DP_IG_HPD)
R9305 100K 5% 1/16W MF-LF 402 (DP_EG_HPD)
R9307 1K 5% 1/10W MF-LF 402 (DP_HPD_R → DP_HOTPLUG_DET)
R9301 10K 5% 1/16W MF-LF 402 (DPMUX_EN_HPD)
C9301 1UF 10% 6.3V CERM-X5R 402 (DPMUX_EN_HPD)
R9302 10K 1% 1/16W MF-LF 402 (DPMUX_EN_PLD)
R9303 0 5% 1/16W MF-LF 402 (DP_MUX_EN)

PP3V3_S0 → DPMUX_EN_S0&DPMUX_EN_PLD
DPMUX_EN_PLD → DP_MUX_EN
DP_HOTPLUG_DET (MAKE_BASE=TRUE)
GND: B3 C8 G8 H4 H7

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0

C9370 0.1UF 20% 16V CERM 402

R9370 20K 5% 1/16W MF-LF 402
R9371 20K 5% 1/16W MF-LF 402
R9372 20K 5% 1/16W MF-LF 402
R9373 20K 5% 1/16W MF-LF 402

U9370 SN74LV4066A QFN1 (VCC, GND THRM)

LVDS_DDC_SEL_EG	C1	A1 ↔ LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	C2	A2 ↔ LVDS_IG_DDC_CLK; B2 ↔ LVDS_DDC_CLK
	C3	A3 ↔ LVDS_EG_DDC_DATA; B3 ↔ LVDS_IG_DDC_DATA
	C4	A4 ↔ LVDS_IG_DDC_DATA; B4 ↔ LVDS_DDC_DATA

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

PAGE TITLE: Muxed Graphics Support

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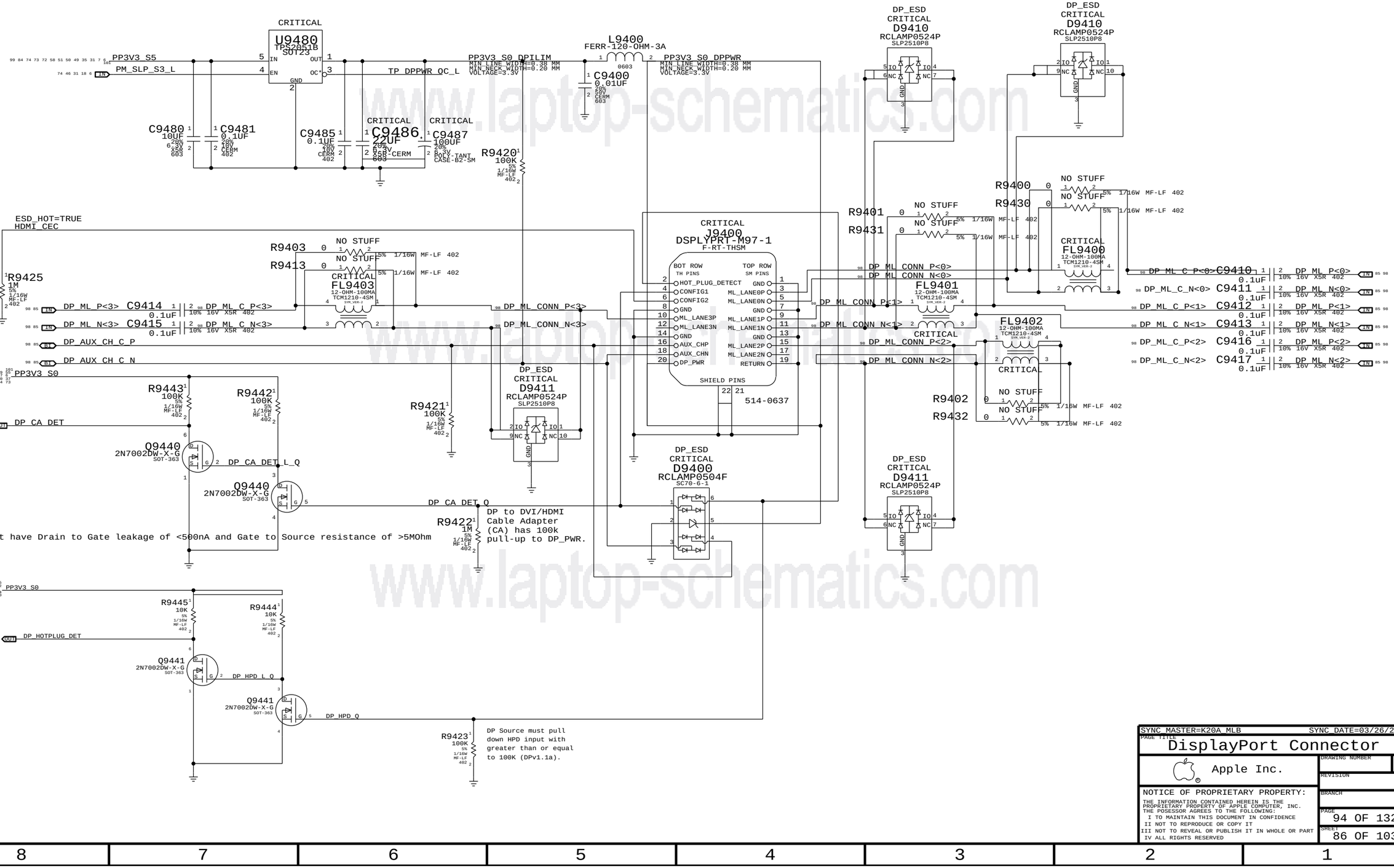
Port Power Switch



SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE: DisplayPort Connector

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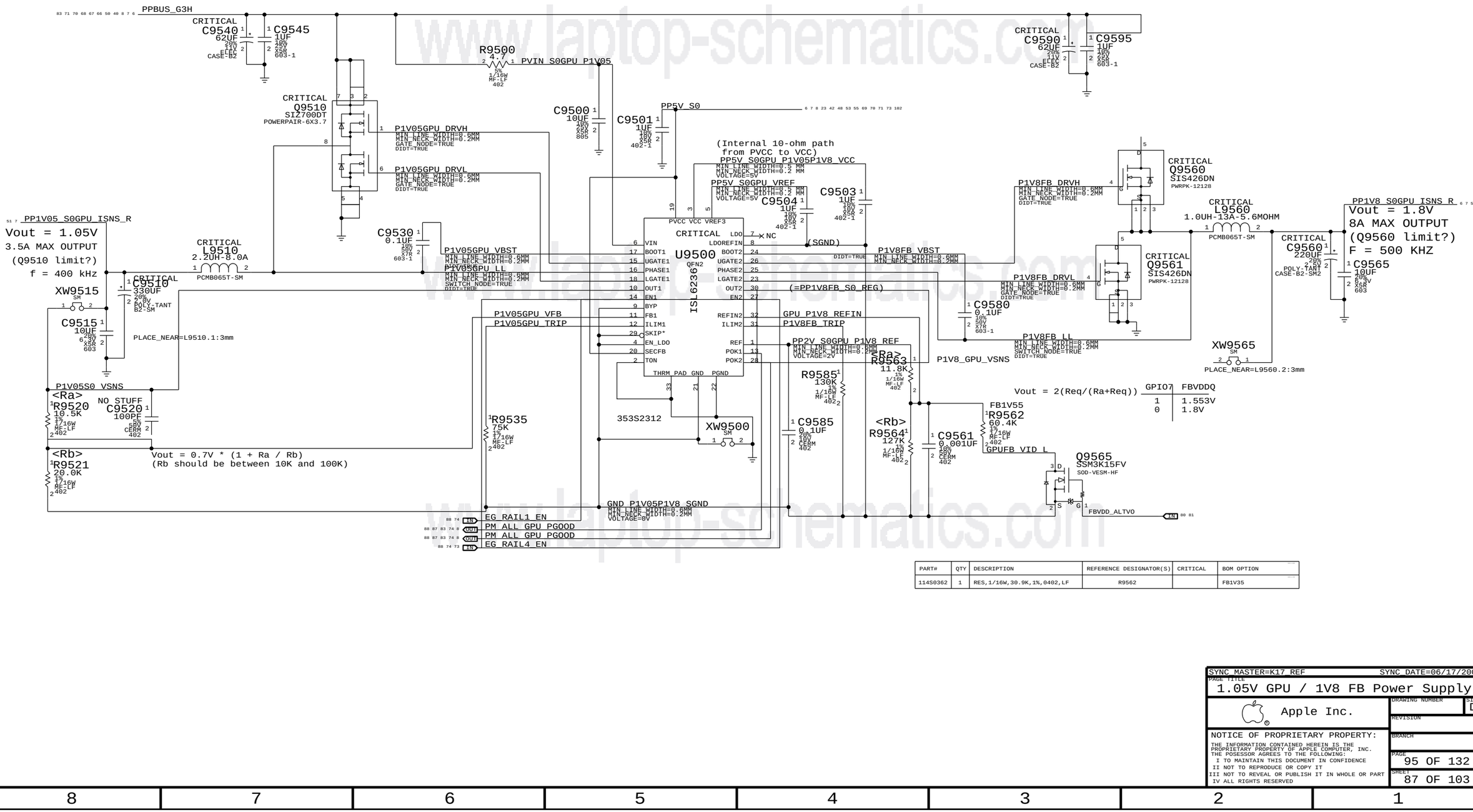

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0362	1	RES,1/16W,30.9K,1%,0402,LF	R9562		FB1V35

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

PAGE TITLE: 1.05V GPU / 1V8 FB Power Supply

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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.E12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

EG_PWRSEQ_EN	R9684	1K	5% 1/16W MF-LF 402
GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402 NO STUFF
EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0

C9610–C9629 0.1UF 20% 10V X5R CERM 402

R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

C9611–C9617 0.1UF 20% 10V X5R CERM 402

C9600 4.7UF 20% 10V X5R 402

C9604–C9609 0.1UF 20% 10V X5R CERM 402

PP1V2_S0

R9640 10K 1% 1/16W MF-LF 402 — PP3V3_S0

R9645 10K 1% 1/16W MF-LF 402

NO STUFF R9641 10K 1% 1/16W MF-LF 402

NO STUFF R9646 10K 1% 1/16W MF-LF 402

R9611 0 5% 1/16W MF-LF 402 — PP1V8_S0 — GMUXPLL_1V8 — PP3V3R1V8_S0_GMUX (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R9612 0 5% 1/16W MF-LF 402 — PP3V3_S0 — GMUXPLL_3V3

L9621 FERR-220-OHM 0402 — PP3V3R1V8_S0_GMUX_ULC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C9631 0.1UF 20% 10V X5R CERM 402

L9620 FERR-220-OHM 0402 — PP3V3R1V8_S0_GMUX_LRC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C9630 0.1UF 20% 10V X5R CERM 402

PP3V3_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)

PP1V8_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V)

VCC: C4 J3 J13 N11 P8 C11
VCCAUX: J2 J14 M8
VCCIO06 B5, VCCIO01 B7, VCCIO02 A12, VCCIO03 C14, VCCIO04 F13, VCCIO05 M12, VCCIO06 M9, VCCIO07 M3, VCCJ N5, M1, C3, F2, K12
ULC_VCCPLL A4
LRC_VCCPLL P11

OMIT CRITICAL
U9600 XP25-5 CSBGA

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	

BANK5

LCD_BKLT_EN	P2	PB7A	
LCD_BKLT_PWM	N2	PB7B	
LVDS_DDC_SEL_EG	P4	PB14A	
LVDS_DDC_SEL_IG	N4	PB14B	
DP_MUX_EN	N3	PB15A	(OD)
DP_MUX_SEL_EG	M4	PB15B	
EG_RESET_L	P5	PB16A	
EG_RAIL1_EN	M5	PB16B	
EG_RAIL2_EN	P6	PB17A	
EG_RAIL3_EN	M6	PB17B	
EG_RAIL4_EN	P7	PB18A	
PEG_CLKREQ_L	M7	PB18B	(OD)
DP_CA_DET_EG	N7	PB19A	
LCD_PWR_EN	N8	PB19B	

BANK4

LPC_AD<0>	P9	PB20A	
LPC_AD<1>	N9	PB20B	
LPC_AD<2>	P10	PB26A	
LPC_AD<3>	M10	PB26B	
LPC_FRAME_L	P12	PB27A	
LPCPLUS_RESET_L	P13	PB27B	
LPC_CLK33M_GMUX	N12	PB28A	
GMUX_INT	P14	PB28B	

BANK7

LVDS_IG_B_DATA_P<2>	B1	PL2A	
LVDS_IG_B_DATA_N<2>	B2	PL2B	
GMUX_PL6A	C2	PL6A	
TP_GMUX_PL6B	D3	PL6B	
LVDS_IG_A_DATA_P<0>	D1	PL7A	
LVDS_IG_A_DATA_N<0>	E1	PL7B	
LVDS_IG_A_DATA_P<1>	D2	PL8A	
LVDS_IG_A_DATA_N<1>	E3	PL8B	
LVDS_IG_A_DATA_P<2>	F1	PL9A	
LVDS_IG_A_DATA_N<2>	G1	PL9B	
LVDS_IG_B_DATA_P<0>	F3	PL10A	
LVDS_IG_B_DATA_N<0>	G2	PL10B	
LVDS_IG_B_DATA_P<1>	H2	PL11A	
LVDS_IG_B_DATA_N<1>	G3	PL11B	
LVDS_IG_A_CLK_P	H1	PL12A	
LVDS_IG_A_CLK_N	H3	PL12B	

BANK6

TP_LVDS_MUX_SEL_EG	L1	PL14A	
TP_GMUX_PL14B	L3	PL14B	
GMUX_RESET_L	K3	PL15A	
GMUX_VSYNC	L2	PL15B	
PM_ALL_GPU_PGOOD	N1	PL25A	
PEX_CLKREQ_L	P1	PL25B	

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1 B8 C6 C12 C13 C14 M14 N10 N6 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

BANK0

PT7A	A2	LVDS_B_DATA_P<0>	OUT
PT7B	A3	LVDS_B_DATA_N<0>	OUT
PT8A	A1	LVDS_B_DATA_P<1>	OUT
PT8B	B3	LVDS_B_DATA_N<1>	OUT
PT9A	C5	LVDS_B_DATA_P<2>	OUT
PT9B	A5	LVDS_B_DATA_N<2>	OUT
PT14A	B6	EG_PWRSEQ_EN	IN
PT14B	C7	GMUX_DEBUG_RESET_L	IN
PT15A	A6	LVDS_A_CLK_P	OUT
PT15B	A7	LVDS_A_CLK_N	OUT
PT16A	C8	LVDS_B_CLK_P	OUT
PT16B	C9	LVDS_B_CLK_N	OUT
PT17A	A8	LVDS_A_DATA_P<0>	OUT
PT17B	B9	LVDS_A_DATA_N<0>	OUT
PT18A	A9	LVDS_A_DATA_P<1>	OUT
PT18B	C10	LVDS_A_DATA_N<1>	OUT
PT19A	B10	LVDS_A_DATA_P<2>	OUT
PT19B	A10	LVDS_A_DATA_N<2>	OUT
PT20A	A11	GND	
PT20B	B12	GND	
PT28A	B13	GND	
PT28B	A13	GND	

BANK1

BANK2

PR2A	A14	DP_CA_DET	IN
PR2B	B14	DP_HOTPLUG_DET	IN
PR6A	D12	LVDS_EG_A_DATA_P<0>	IN
PR6B	D13	LVDS_EG_A_DATA_N<0>	IN
PR7A	D14	LVDS_EG_A_DATA_P<1>	IN
PR7B	E14	LVDS_EG_A_DATA_N<1>	IN
PR8A	E12	LVDS_EG_A_DATA_P<2>	IN
PR8B	F12	LVDS_EG_A_DATA_N<2>	IN
PR9A	F14	LVDS_EG_B_DATA_P<0>	IN
PR9B	G14	LVDS_EG_B_DATA_N<0>	IN
PR10A	G12	LVDS_EG_B_DATA_P<1>	IN
PR10B	G13	LVDS_EG_B_DATA_N<1>	IN
PR11A	H13	LVDS_EG_B_DATA_P<2>	IN
PR11B	H12	LVDS_EG_B_DATA_N<2>	IN
PR12A	H14	LVDS_EG_A_CLK_P	IN
PR12B	J12	LVDS_EG_A_CLK_N	IN
PR14A	L14	LVDS_IG_PANEL_PWR	IN
PR14B	M13	EG_LCD_PWR_EN	IN
PR24A	N14	LVDS_IG_BKL_ON	IN
PR24B	N13	EG_BKLT_EN	IN

BANK3

EG_RAIL1_EN, EG_RAIL2_EN, EG_RAIL3_EN, EG_RAIL4_EN, LCD_PWR_EN

R9678 4.7K 5% 1/16W MF-LF 402
R9671 4.7K 5% 1/16W MF-LF 402
R9672 4.7K 5% 1/16W MF-LF 402
R9673 4.7K 5% 1/16W MF-LF 402
R9674 4.7K 5% 1/16W MF-LF 402

GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/16W MF-LF 402

PP3V3_S3 — R9676 100K 5% 1/16W MF-LF 402 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563

ALL_SYS_PWRGD

CRITICAL J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	20 88
3	JTAG_GMUX_TDI	19 88
4	JTAG_GMUX_TMS	19 88
5		
6	JTAG_GMUX_TCK	20 25 88
7		
8		

NO STUFF R9647 10K 1% 1/16W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/24/2009

PAGE TITLE: Graphics MUX (GMUX)

Apple Inc.

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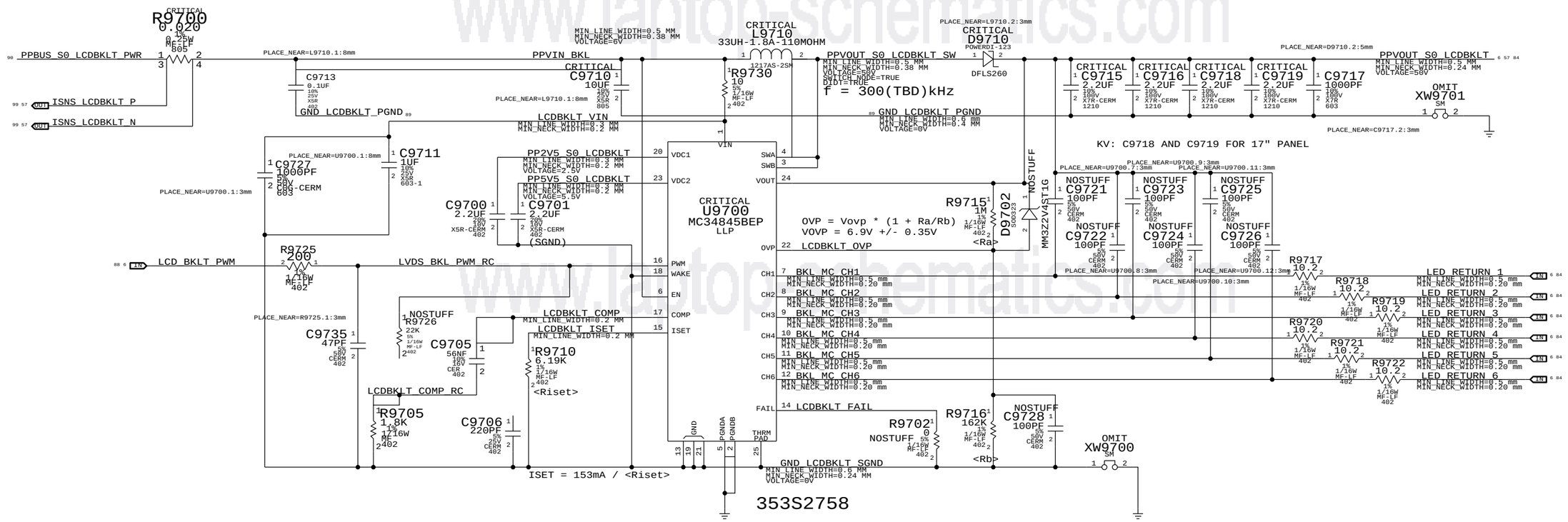

PLACEMENT_NOTE=PLACE XW9700 FAR FROM THE NOISY PINS 3 AND 4

17 Inch Panel (14 LEDs per string)

Target: ISET = 25mA, OVP = 50V
ACTUAL: ISET = 24.7mA, OVP = 49.5V

KV: WAKE AND EN WIRING CHANGED FROM REF SCHEMATIC AS QFET IS PRESENT ON P.98

SYNC_MASTER=K17_VEMURI SYNC_DATE=12/16/2009

PAGE TITLE: LCD Backlight Driver (MC34845)

Apple Inc.

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CRITICAL

Q9806
FDC638APZ_SBMS001 PPBUS S0 LCDBkLT FET
SSOT6-HF

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

F9800
3AMP-32V-467
603-HF

PPVIN_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=10V

R9808 301K 1% 1/16W MF-LF 402
C9802 0.1UF 10% 16V X5R 402
PBUS_S0_LCDBKLT_EN_DIV
R9809 147K 1% 1/16W MF-LF 402
PBUS_S0_LCDBKLT_EN_L

Q9807
SSM6N15FEAPE
SOT563

LCD_BKLT_EN
R9840 4.7K 5% 1/16W MF-LF 402
BKLT_EN_L

Q9807
SSM6N15FEAPE
SOT563

BKLT_PLT_RST_L

PPBUS_S0_LCDBKLT_PWR
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=10V

SYNC_MASTER=K20A_MLB SYNC_DATE=03/26/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 71
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 47
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 47
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 47 69
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 47
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 69
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 69
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 70
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 70
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 70
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 70
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	75
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	75
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 75
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 9 75
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	75
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	75

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0> 11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1> 11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2> 11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3> 11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4> 11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5> 11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6> 11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7> 11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0> 11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1> 11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2> 11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3> 11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4> 11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5> 11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6> 11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7> 11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8 85
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 18 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 18 85
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 88
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	17 42
	SATA_90D	SATA	SATA_HDD_D2R_N	17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	17 42
	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	17 42
	SATA_90D	SATA	SATA_ODD_D2R_N	17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
SATA_EXTA_R2D	SATA_90D	SATA	TP_SATA_EXTA_R2D_C_P	8 17
	SATA_90D	SATA	TP_SATA_EXTA_R2D_C_N	8 17
SATA_EXTA_D2R	SATA_90D	SATA	TP_SATA_EXTA_D2R_P	8 17
	SATA_90D	SATA	TP_SATA_EXTA_D2R_N	8 17
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATA_ICOMP	
USB_EXTA	USB_85D	USB	USB_EXTA_P	36 43
	USB_85D	USB	USB_EXTA_N	36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	35 43
	USB_85D	USB	USB_EXTB_N	35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	35 44
	USB_85D	USB	USB_EXTC_N	35 44
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	19 36
	USB_85D	USB	USB_HUB2_UP_N	19 36
USB_MINI	USB_85D	USB	NC_USB_MINIP	6
	USB_85D	USB	NC_USB_MININ	6
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	19 35
	USB_85D	USB	USB_HUB1_UP_N	19 35
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	33 35
	USB_85D	USB	USB_CAMERA_N	33 35
USB_BT	USB_85D	USB	USB_BT_P	33 36
	USB_85D	USB	USB_BT_N	33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	36 54
	USB_85D	USB	USB_TPAD_N	36 54
USB_IR	USB_85D	USB	USB_IR_P	35 45
	USB_85D	USB	USB_IR_N	35 45
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 34 36
	USB_85D	USB	USB_EXCARD_N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	19 103
	USB_85D	USB	USB_BRCRYPT_N	19 103
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 46 48 88
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 46 48 88
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 48 88
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 46
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 48
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 17 25 26 28 30 32 34 42 48 49 64
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	6 17 25 26 28 30 32 34 42 48 49 64
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 49
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 49
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 49
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 49
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 59
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 59
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 59
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 59
	HDA_50S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 59
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 47
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 48
	SPI_55S	SPI	SPI_CLK	48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 48
	SPI_55S	SPI	SPI_MOSI	48
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 48
	SPI_55S	SPI	SPI_CS0_L	48
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 34
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 34
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	17 34
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	17 34
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 17 34
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 17 34
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 75
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 75
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 34
1231	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
1232	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
1233	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
1234	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
1235	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1236	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1237	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
1238	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
1239	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
1240	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
1241	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
1242	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
1243	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
1244	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
1245	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
1246	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20
1247	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
1248	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
1249	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
1250	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	

SYNC_MASTER=K17_REF SYNC_DATE=06/17/2009

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI 27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO 27 37
	ENET_50S	ENET_3X	ENET_RESET_L 27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0> 37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0> 37 38

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 40 41
Port 2 Not Used				

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 33 46 49 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 33 46 49 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	46 49 52
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	46 49 52
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 46 49 65 66
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 46 49 65 66
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	46 49 57 102
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	46 49 57 102

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	66
	1TO1_DIFFPAIR		CHGR_CSI_N	66
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	66
	1TO1_DIFFPAIR		CHGR_CSO_N	66

SYNC_MASTER=K17_WFERRY SYNC_DATE=06/09/2009

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	85 88
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	85 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	85 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	85 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	85 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	85 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	85 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	85 88
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 84
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 84
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	84 85
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	84 85
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 84 85
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 84 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	84 85
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	84 85
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 84 85
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 84 85
DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0>	86
DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0>	86
DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0>	85 86
	DP_85D	DISPLAYPORT	DP_ML_N<3..0>	85 86
DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>	86
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>	86
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P	85 86
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N	85 86

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	77 78
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	77 78
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	77 78
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	77 78
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	77 78
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE	77 78
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE	77 78
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L	77 78
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	77 78
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	77 78
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	77 78
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	77 78
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	77 78
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	77 78
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	77 78
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	77 78
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	77 78
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	77 78
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	77 78
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	77 78
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	77 78
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	77 78
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	77 78
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	77 78
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	77 78
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	77 78
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	77 78
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	77 78
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	77 78
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	77 78
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	77 78
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	77 78
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	77 78
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	77 78
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	77 78
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	77 78
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	77 78
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	77 78
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	77 78
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	77 78
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	77 78
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	77 78
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	77 78

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
(CK505_DATA0)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	27 80 81
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	80 81
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	82 88
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	82 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	82 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	82 88
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	81 82
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	81 82
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	82 88
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	82 88
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	81 82
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	81 82
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0>	82 85
DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0>	82 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P	82 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N	82 85
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P	85
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N	85

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	77 79
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	77 79
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	77 79
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	77 79
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	77 79
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE	77 79
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE	77 79
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L	77 79
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	77 79
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	77 79
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	77 79
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	77 79
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	77 79
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	77 79
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	77 79
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	77 79
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	77 79
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	77 79
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	77 79
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	77 79
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	77 79
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	77 79
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	77 79
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	77 79
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	77 79
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	77 79
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	77 79
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	77 79
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	77 79
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	77 79
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	77 79
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	77 79
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	77 79
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	77 79
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	77 79
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	77 79
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	77 79
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	77 79
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	77 79
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	77 79
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	77 79
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	77 79
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	77 79

SYNC_MASTER=K17 WFERRY SYNC_DATE=06/09/2009

PAGE TITLE: GPU (GT216) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K17 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_R2D_UF_P	42
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	42
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_HDD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_R2D_UF_P	42
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	42
L30D	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P	42
L30C	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N	42
L30F	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P	42
L30B	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N	42
L30G	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P	42
L31C	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N	42
L31A	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P	42
L31E	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N	42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	52
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	52
L28J SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 52
L28H	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 52
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	52
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	52
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	52 80 81
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	52 80 81
SENSE_DIFFPAIR	SENSE_1TO1_55S	THERM	ISNS_3V3_S3_R_P	102
	SENSE_1TO1_55S	THERM	ISNS_3V3_S3_R_N	102
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	33 57 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	33 57 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	57
	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	51
	SENSE_1TO1_55S	SENSE	GPUISENS_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	33 57 99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	33 57 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	57
	SENSE_1TO1_55S	SENSE	DDRISNS_N	57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	51
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	42 57
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	42 57
L24J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	57
L25C	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	57
L24G SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	57
L25A	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	57
L25G SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	42 57
L25E	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	42 57
L25C SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	57 89
L25A	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	57 89
L23G SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NC_ISNS_P1V05S0PCH_P	8 50
L24C	SENSE_1TO1_55S	SENSE	NC_ISNS_P1V05S0PCH_N	8 50
L23J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	71
L23F	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	71
L23E SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_R_P	71
L23C	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_R_N	71
L23A SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NC_ISNS_P3V3S0MPCH_P	8 102
L24E	SENSE_1TO1_55S	SENSE	NC_ISNS_P3V3S0MPCH_N	8 102
L25E SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P3V3S0MPCH_R_P	102
L26C	SENSE_1TO1_55S	SENSE	ISNS_P3V3S0MPCH_R_N	102
L29J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P	70
L29F	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N	70
L29C SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P	50 70
L28H	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N	50 70
L27J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_R_P	102
L27F	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_R_N	102
L27C SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NC_ISNS_PVTTS0PCH_P	8 102
L27A	SENSE_1TO1_55S	SENSE	NC_ISNS_PVTTS0PCH_N	8 102
L27G SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PVTTS0PCH_R_P	102
L27E	SENSE_1TO1_55S	SENSE	ISNS_PVTTS0PCH_R_N	102
L27J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_P	51
L27F	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_N	51
L27C SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	102
L28C	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	102
L28J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	51
L28F	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	51
L28E SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	102
L28A	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	102
L28G SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	51
L28E	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	51
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	51 68
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	51 68
SENSE_DIFFPAIR	SENSE_1TO1_55S	THERM	ISNS_1V5_S3_R_P	51
	SENSE_1TO1_55S	THERM	ISNS_1V5_S3_R_N	51
L29J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	57
L29F	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	57
L30J SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	83
L30F	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	83
L30D SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P	50
L30B	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N	50

K17 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P	66
	1TO1_DIFFPAIR		CHGR_CSI_R_N	66
	1TO1_DIFFPAIR		CHGR_CSO_R_P	59 66
	1TO1_DIFFPAIR		CHGR_CSO_R_N	59 66
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 43
(USB_EXTD)	USB_85D	USB	USB_BRCRYPT_CONN_P	
(USB_EXTD)	USB_85D	USB	USB_BRCRYPT_CONN_N	
(USB_CAMERA)	USB_85D	USB	USB_CAMERA_CONN_P	6 33
(USB_CAMERA)	USB_85D	USB	USB_CAMERA_CONN_N	6 33
	USB_85D	USB	CONN_USB2_BT_P	6 33
	USB_85D	USB	CONN_USB2_BT_N	6 33
	USB_85D	USB	USB_LT2_P	6 43
	USB_85D	USB	USB_LT2_N	6 43
	USB_85D	USB	USB2_EXCARD_CONN_P	6 34
	USB_85D	USB	USB2_EXCARD_CONN_N	6 34
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	85
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	85
L31C	USB_85D	USB	USB_BRCRYPT_R_P	
L31E	USB_85D	USB	USB_BRCRYPT_R_N	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 34
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_FL_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_FL_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_BL_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_BL_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_FR_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_FR_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_BR_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_BR_OUT_N	6 62 63
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	6 62 63
	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	6 62 63
L41C	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_C_P	62
L41E	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_C_N	62
L41J	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_C_P	62
L41G	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_C_N	62
L41L	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_C_P	62
L41N	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_C_N	62
L42J	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_C_P	62
L42G	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_C_N	62
L42L	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_C_P	62
L42N	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_C_N	62
L42C	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_L_P	62
L42E	DIFFPAIR	AUDIO	SPKRAMP_FL_IN_L_N	62
L42A	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_L_P	62
L42G	DIFFPAIR	AUDIO	SPKRAMP_BL_IN_L_N	62
L42E	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_L_P	62
L43J	DIFFPAIR	AUDIO	SPKRAMP_FR_IN_L_N	62
L43C	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_L_P	62
L43E	DIFFPAIR	AUDIO	SPKRAMP_BR_IN_L_N	62
L43A	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_L_P	62
L43G	DIFFPAIR	AUDIO	SPKRAMP_LFE_IN_L_N	62
L43E	DIFFPAIR	AUDIO	SSM2315FL_IN_P	62
L43C	DIFFPAIR	AUDIO	SSM2315FL_IN_N	62
L43J	DIFFPAIR	AUDIO	SSM2315FR_IN_P	62
L43L	DIFFPAIR	AUDIO	SSM2315FR_IN_N	62
L43N	DIFFPAIR	AUDIO	SSM2315BR_IN_P	62
L44C	DIFFPAIR	AUDIO	SSM2315BR_IN_N	62
L44A	DIFFPAIR	AUDIO	INT_MIC_F_P	63 64
L44G	DIFFPAIR	AUDIO	INT_MIC_F_N	63 64
L44E	DIFFPAIR	AUDIO	INT_MIC_P	6 63
L44C	DIFFPAIR	AUDIO	INT_MIC_N	6 63
L44E	DIFFPAIR	AUDIO	SSM2315BL_IN_P	62
L44G	DIFFPAIR	AUDIO	SSM2315BL_IN_N	62
L44J	DIFFPAIR	AUDIO	SSM2315LFE_IN_P	62
L44L	DIFFPAIR	AUDIO	SSM2315LFE_IN_N	62
	USB_85D	USB	USB_TPAD_R_P	54
	USB_85D	USB	USB_TPAD_R_N	54
	USB_85D	USB	USB_LT3_P	6 44
	USB_85D	USB	USB_LT3_N	6 44
		SB_POWER	PP3V3_S5	84 85 101 6 7 31 35 49 50 51 58 72 73 74
		SB_POWER	PP3V3_S0	69 70 71 72 73 74 81 84 85 86 6 7 8 25 26 27 28 30 34 37 40 42 47 48 49 52 53 55 59 63 64 80 101
		SB_POWER	PP1V5_S0	34 42 59 72 74
		GND	GND	

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Project Specific Constraints

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K17 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?

NOTE: From T18 MLB, changed to reflect K17 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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PCH "S0" Rails

XWC100 SM
PPCPUVTT_S0 — 4759 mA
PP1V05_S0_PCH — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=1.05V; MAKE_BASE=TRUE
PP1V05_S0_PCH — 128 mA (0 mA if PCH_VRM_YES?)
PP1V05_S0_PCH — 1432 mA
PP1V05_S0_PCH — 137 mA
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH
PP1V05_S0_PCH — 3062 mA
PP1V05_S0_PCH — 1849 mA S0, 700 mA M-on

PCH "S0M" Rails

XWC110 SM
PPCPUVTT_S0 — 62 mA
PPVTT_S0_PCH — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.05V; MAKE_BASE=TRUE OR 1.1V
PPVTT_S0_PCH — < 1 mA
PPVTT_S0_PCH — 61 mA (1.1V)
PPVTT_S0_PCH — 58 mA (1.05V)

XWC120 SM
PP1V8_S0 — 250 mA
PP1V8_S0_PCH — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.8V; MAKE_BASE=TRUE
PP1V8_S0_PCH — 59 mA
PP1V8_S0_PCH — 35 mA
PCH_NAND_1V8
RC125 0 5% 1/10W MF-LF 603
PP3V3R1V8_S0_PCH_VCCPNAND — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=3.3V; MAKE_BASE=TRUE OR 1.8V
PP3V3R1V8_S0_PCH_VCCPNAND — 156 mA (1.8V); ??? mA (3.3V); WF: Estimate 300 mA for budget purposes
PCH_NAND_3V3
RC126 0 5% 1/10W MF-LF 603

XWC130 SM
PP3V3_S0 — 729 mA
PP3V3_S0_PCH — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=3.3V; MAKE_BASE=TRUE
PP3V3_S0_PCH — < 1 mA
PP3V3_S0_PCH — < 1 mA
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH — 357 mA
PP3V3_S0_PCH
PP3V3_S0_PCH
PP3V3_S0_PCH — 69 mA

XWC135 SM NO STUFF
RC136 0 5% 1/10W MF-LF 402
PP3V3_S0_PCH_VCCALVDS — MIN_LINE_WIDTH=0.2 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=3.3V; MAKE_BASE=TRUE
PP3V3_S0_PCH_VCCALVDS — < 1 mA

XWC140 SM
PP3V3_S0 — 6 mA
PP3V3R1V5_S0_PCH — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.5V; MAKE_BASE=TRUE OR 3.3V
PP3V3R1V5_S0_PCH — 6 mA (3.3V)

PCH "S5" Rail

XWC150 SM
PP3V3_S5 — 165 mA
PP3V3_S5_PCH — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=3.3V; MAKE_BASE=TRUE
PP3V3_S5_PCH — ≤ 1 mA S0-S5
PP3V3_S5_PCH — ≤ 1 mA S0-S5
PP3V3_S5_PCH — 163 mA S0 /
PP3V3_S5_PCH — 65 mA S3-S5

XWC170 SM
PP3V3_S0 — 85 mA
PP3V3_S0M_PCH — MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=3.3V; MAKE_BASE=TRUE
PP3V3_S0M_PCH — 85 mA S0, 22 mA M-on

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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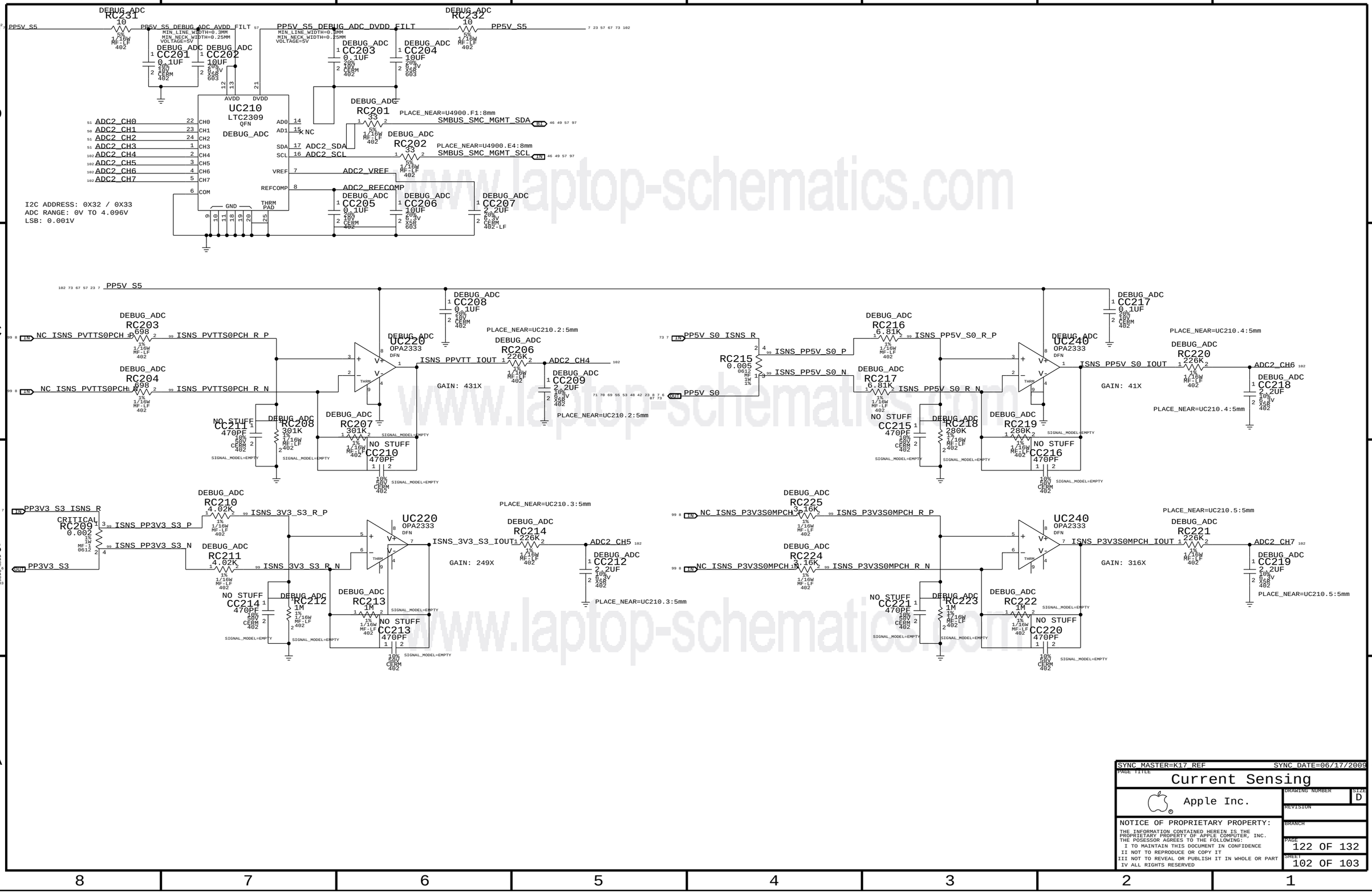

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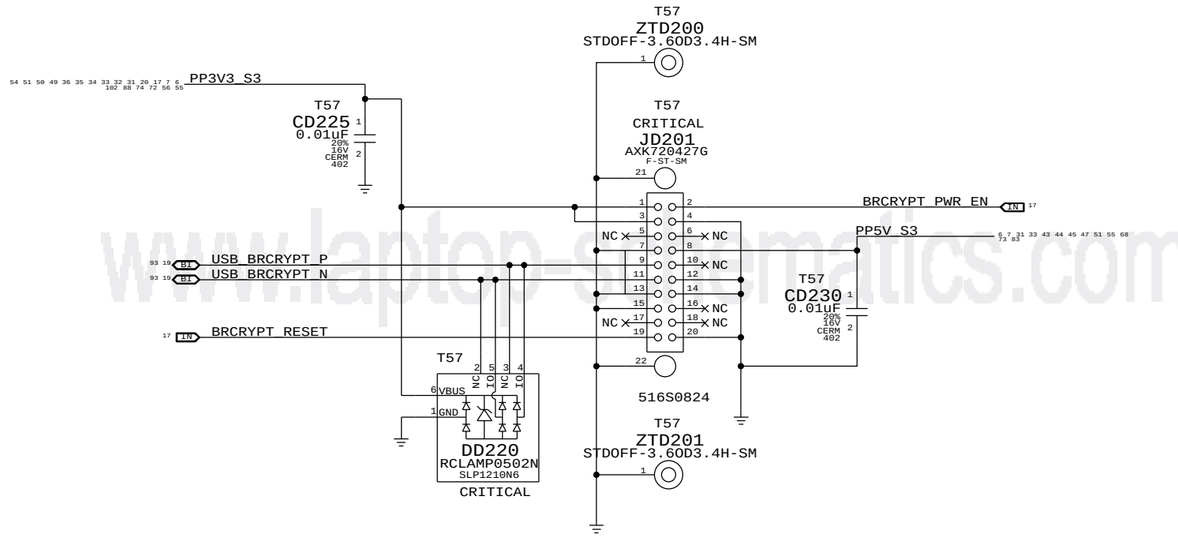

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